89601564

02

CONTROL DATA CORPORATION

CDC® PAPER TAPE READER/ PAPER TAPE PUNCH/CARD PUNCH CONTROLLER AND PAPER TAPE RELAY STATION

FE516-A, DK609-A

GENERAL INFORMATION
PROGRAMMING
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
LOGIC DESCRIPTION
MAINTENANCE

HARDWARE REFERENCE/MAINTENANCE MANUAL

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MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
FE516	01	ECO CK1770	Serial Number 51
DK609	01	ECO CK1770	Serial Number 51

PREFACE

This manual describes the operation and maintenance of the CONTROL DATA FE516-A Paper Tape Reader/Paper Tape Punch/Card Punch and the DK609-A Paper Tape Relay Station.

It is assumed that the reader of this book is already familiar with the CONTROL DATA Cyber 18 micro-programmable processor, has had 6 months training in digital computers,and is familiar with data communications.

Other related documents which may be useful to the reader are listed below.

Title	Publication No.
Microprocessor Reference Manual	88973500
1700 Computer System	60153100
Basic Micro-Programmable Hardware Maintenance Manual	39451400
FE516-A Field Print Package	89600274
DK609-A Field Print Package	89601565
Cyber 18-20/30 Timeshare Computer System Hardware Maintenance Manual, Volumes 1 and 2.	96769302

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TABLES

GENERAL INFORMATION

INTRODUCTION

The manual describes the Paper Tape Reader, Paper Tape Punch, and Card Punch (PT/CP) Controller for the Cyber 18 compter.

The Controller interfaces with the Computer via the AQ channel with the Facit Paper Tape Reader, Facit Paper Tape Punch, and CDC 9290 Card Punch devices.

The Controller consists of one PWA module plugged into an AQ only card slot in the Cyber 18 mainframe. A Paper Tape Relay Station is required to interface the Paper Tape Reader and Punch devices with the Controller and the paper tape devices must be equipped with the Facit SP1 interface.

The Controller has the following characteristics:

- The logic uses the concept of microprocessing.
- interfaces the Facit 4020/4070 Paper Tape devices equipped with SP1 interface via an external PT Relay Station.
- interfaces the CDC 9290 Card Punch Device.
- Paper Tape Reader -
  read forward and reverse,
  program selectable 8 to 16 bit assembly or 8 bit data transfer to lower of A-Register,
  transfer function and status to/from devices.
  error detection using odd parity
- Paper Tape Punch
  punch paper tape
  program selectable 16 to 8 bit disassembly or an 8 bit data transfer from the lower 8 bits of the A-register,
  backstepping
  transfer function and status to/from device
- parity generation using odd parity
- Card Punch -
  punch cards,
  Data Transfers from A-Register,
  feed cards,
  offset,
  transfer function and status information to/from device
- The Controller is capapble of handling concurrent separate requiests to and from all three devices.
- One macro interrupt line issued for all three devices.
- The Controller is capable of exercising its internal data paths and most of its control logic withour the devices being active. This process tests 70-8- per cent of the Controller logic and of the PT Relay Station logic.

The Controller is built from TTL logic components mounted on one Cyber 18 board, containing PROM's which are socket mounted. The A/Q card slot where the Controller is plugged-in must not have any "optional" wiring on it.

In addition, three interrupt lines (Pin Nos. 49, 50 and 250) have been pre-wired as peripheral I/O pins. XX is level number assigned per system configuration.

Voltage Requirement

This Controller operates on 5vdc±5%.

Power Requirement

This Controller has a maximum power consumption of 8 amps.

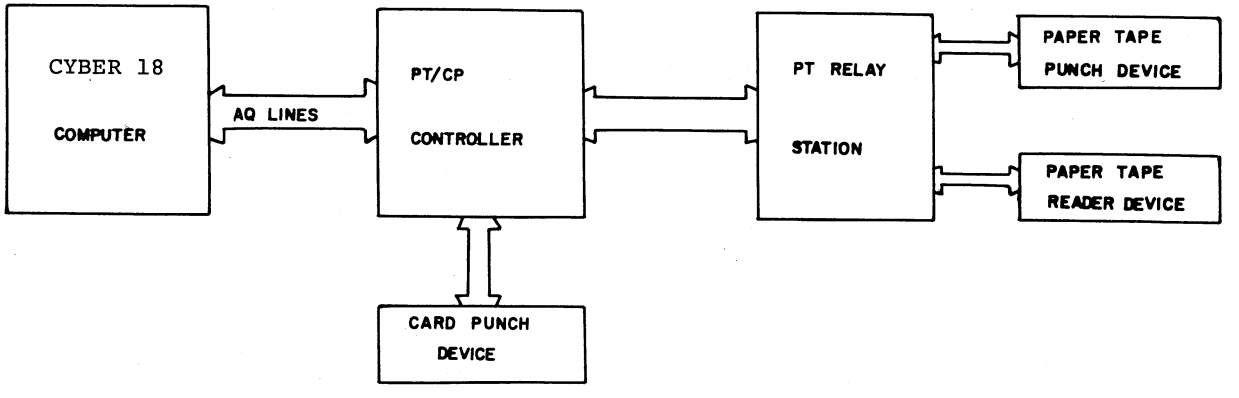


Figure 1-1. Basic System Configuration

PROGRAMMING

PROGRAMMING CONSIDERATIONS

The Q register designates the equipment to be referenced and specifies the operation to be performed upon execution of an INPUT or OUTPUT instruction.

One Equipment Number and different codes are used for referencing each one of the three devices involved.

Figure 2-1 illustrates the Q register format.

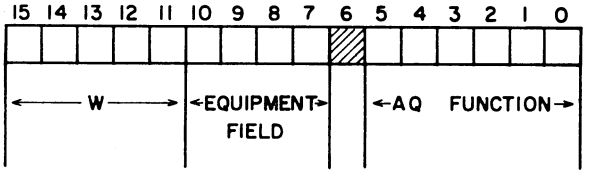


Fig.2-1. Q Register for I/O Instructions

The W Field (bits 15 - 11) must always be zero.

The Equipment Field (bits 10 - 07) selects the Controller. This Field code must match the equipment number setting of the jumper plugs located on the printed board.

Bit Q06 should always be zero.

Bits Q00 through Q05 specify the operation to be performed by the Controller in response to CPU INPUT or OUTPUT instructions.

Table 2-1 shows the available operations and their corresponding codes.

Bit Q04 is always zero, except for Clear Controller and Status - 1 instruction.

Note: There is no Unit Selection. Unit Selection is done by the A/Q function.

Upon receipt of a test-type Output Instruction, the Controller becomes busy, the Busy Status-1 bit is set and remains set until test completion. The Controller becomes busy as well for about 40 µsec (or less) upon receipt of a Clear Controller Command (the Busy bit is set for the duration). When the Busy bit is set, all instructions are rejected by the Controller except Clear Controller and Status-1.

Any time one of the test-type AQ instructions is issued (any CPU Output or Input instruction with Q03 = 1, Q04 = 0 and Q05 = 1), the Controller enters a special test-state.

When in the test-state the Controller accepts only test-type AQ input or output instructions, except Clear-Controller and Status-1.

Therefore, when in the test-state, the Controller does not perform operations which are related to the devices.

To exit from the test-state a Clear Controller command must be issued. This command sets the necessary initial conditions for normal operation.

TABLE 2-1. INPUT/OUTPUT INSTRUCTIONS

Q05	Q04	Q03	Q02	Q01	Q00	Output Instruction	Input Instruction
Ø	1	Ø	Ø	Ø	Ø	Clear Controller	Status -1
0	0	1	0	0	0	PTR START/STOP	CP Status 2
0	0	1	0	0	1	PTR FORWARD/BACKWARD	CP Status 3
0	0	1	0	1	0	PTR CLEAR	CP Status 4
0	0	1	0	1	1	PTR CLEAR INTERRUPT	CP Status 5
0	0	1	1	0	0	PTR INTERRUPT REQUEST	Illegal*
0	0	1	1	0	1	PTR DATA MODE (CHAR./ASSY)	Illegal*
0	0	1	1	1	0	Illegal	Illegal*
0	0	1	1	1	1	Illegal (Reject	Illegal*
1	0	0	0	0	0	PTP START/STOP	Illegal*
1	0	0	0	0	1	PTP DEVICE FUNCTION	Illegal*
1	0	0	0	1	0	PTP DATA	Illegal*
1	0	0	0	1	1	PTP CLEAR	Illegal*
1	0	0	1	0	0	PTP CLEAR INTERRUPT	Illegal*
1	0	0	1	0	1	PTP INTERRUPT REQUEST	Illegal*
1	0	0	1	1	0	PTP DATA MODE(CHAR./DISASSY)	Illegal*
1	0	0	1	1	1	Illegal (Reject)	Illegal*
0	0	0	0	0	0	Illegal (Reject)	Illegal*
0	0	0	0	0	1	Illegal (Reject	Illegal*
0	0	0	0	1	0	CP FEED	Illegal (Reject)
0	0	0	0	1	1	CP CLEAR	Illegal (Reject)
0	0	0	1	0	0	CP CLEAR INTERRUPT	PTR READ DATA
0	0	0	1	0	1	CP INT REQUEST	PTR ASSY. TRANSTER STATION (1=Not Completed; 0=Completed)
0	0	0	1	1	0	CP OFFSET	PTR ALARM STATUS
0	0	0	1	1	1	CP DATA	PTP DISASSY. TRANSFER STATION (1=Not Completed; 0=Completed)
1	0	1	0	0	0	Self Test 1 (Data Path)	Illegal*
1	0	1	0	0	1	Self Test 2 (FF's and Jumps)	Illegal*
1	0	1	0	1	0	Self Test 3 (I/O Station (Echo)	Illegal*

TABLE 2-1 INPUT/OUTPUT INSTRUCTIONS (CONT'D.)

Q05	Q04	Q03	Q02	Q01	Q00	Output Instruction	Input Instruction
1	0	1	0	1	1	TEST MODE LOAD FILE ADDRESS	Illegal*
1	0	1	1	0	0	TEST MODE INT RQST	Illegal (Reject)
1	0	1	1	0	1	TEST MODE CLEAR INT	Illegal (Reject)
1	0	1	1	1	0	Illegal (Reject)	A-OUT TEST STATUS
1	0	1	1	1	1	Illegal (Reject)	TEST READ FILE

* The PT/CP Controller will reply to these functions; A-line data, however, will not be valid.

NOTE: Ø can be either 1 or 0.

Common Functions

These functions apply to all three devices.

Clear Controller

This function is initiated by a WRITE signal with Q bits coded as shown in Table 2-1.

This function is always accepted by the Controller unless a protect violation occurs.

It clears all internal logic FF's, registers, File registers, interrupt requests and response.

For the Paper Tape Reader Logic: Data Status FF becomes reset, reading is set in forward direction, character mode and Stop conditions are set. Assembly transfer status FF and PTR Transfer Parity Error FF are reset.

For the Paper Tape Punch Logic: Data Status FF becomes reset, Character mode and Stop condition are set. Disassembly transfer status FF and PTP CA FF are reset.

For the Card Punch Logic: Data Status FF, Info Ready, Feed Command and CP Offset become reset. The On Bus FF is constantly set and is therefore not affected. Upon receipt of this command, the Controller becomes busy and remains busy for 40 sec (or less).

Status-1 A-Register bits after this command is issued, look as follows:

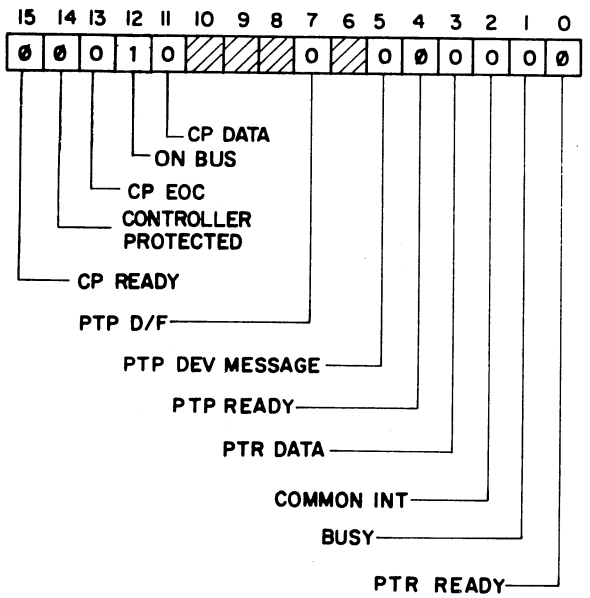


Fig.2-2. Status-1 A-Register Bits after Clear Controller

Note that the value of bits 00, 04, and 15 depend on each device status. The value of bit 14 depends on the corresponding jumper position (UPO).

Status-1

This function is initiated by a READ signal with Q-bits coded as shown in Table 2-1.

This function is accepted at any time. It is used to monitor operating conditions of the Controller and devices.

The status information is loaded into the A-Register as shown in Figure 2-3

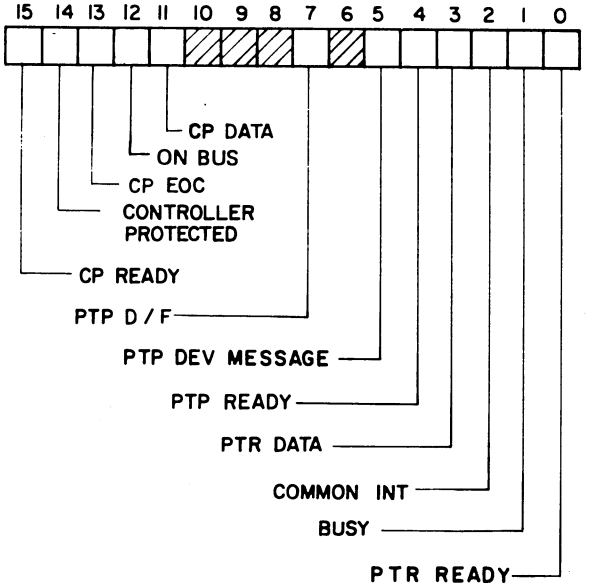


Fig. 2-3. Status-1, A-Register Bits

Bits 6, 8, 9 and 10 are ignored by the CPU.

PTR Ready (A00 = 1)

The Paper-tape Reader is connected and Ready.

The Paper-tape Reader red ERROR lamp lights and the device becomes Not-Ready if one of the following conditions occurs:

1. From the time when the DC voltage is turned on until the START control is actuated, thereby making certain that the proper initial conditions for reading are established.

2. When tape is fed using the FEED control, thereby indicating that the tape is being fed without being read.

4. If an attempt is made to start reading without having inserted tape into the reader.

5. If, for any reason, the tape is under excessive tension. Example: at the end of a tape that is taped to the coil core.

6. When the tape-feed distance stepped for each character is too short, when tape feed is too low, etc. That is to say, when the internal monitoring system that ensures proper feeding and reading issues an alarm.

   At the time that the PTR device becomes Not-ready, the PTR Data Status bit and the PTR AC signal are reset.

Busy (A01 = 1)

The Controller becomes busy during execution of a Self-Test command or during a Clear Controller command. When executing a Self-Test command, the Controller remains busy until test completion. When executing a Clear Controller command, the Controller remains Busy for 40 µsec.

When the Busy bit is set, all AQ instructions are rejected except Clear Controller and Status-1 requests.

Common Interrupt (A02 = 1)

This bit indicates that a common interrupt response was generated by the Controller. Other bits of Status-1 must be monitored to determine which device caused the interrupt and what caused the interrupt.

Note that each one of the three devices has its own independent interrupt. These three lines are "ORed" and the resulting interrupt line is connected to the back plane on the MP mainframe. This bit is cleared by a PTR, PTP, or CP Clear Interrupt command if an interrupt exists only for the corresponding device.

PTR Data (A03 = 1)

This bit indicates when set that the Controller received PTR data and that an AQ data transfer operating may be performed. The Data Status bit is reset after a PTR Read Data instruction is issued by the CPU.

This bit is cleared by PTR Clear, Clear Controller, and Master Clear.

A necessary condition for this bit to be set is the PTR to be in START condition. PTR STOP condition will not reset this bit.

PTP Ready (A04 = 1)

This bit indicates that the Paper Tape Punch device is connected and ready.

The device becomes Not-ready when the tape is tight or broken. At the time that the PTP device becomes Not-ready, the PTP Data status bit and PTP SC signal are reset.

PTP Device Message (A05 = 1)

The device message status bit is related to the device interface line PTP AM and indicates, when set, that

a) the device has a message to be transmitted, (this occurs normally when the device has detected an error after performing a punch data operation).

b) the device signals a positive answer to the last question posed by the CPU in the form of a PTP Function Code instruction.

The device message may indicate that one or more of the following occurred:

Tape Low - this is an option feature of the the device,

Echo Error- Echo check failure sensed by the device on the last punched character.

Parity Error- Parity error on received date sensed.

The device message status bit is valid (whether set or reset) only when the Data Function bit is set. It is updated after every punched data character. It is cleared when the device answer is negative or when there is no message to transmit after punching a character.

PTP Data/Function (A07 = 1)

This bit indicates that the PTP logic of the Controller is ready to receive a Data or a Function word for the Paper Tape Punch device. An AQ Data transfer operation may be performed.

This bit is reset by reply to PTP Data or PTP Device Function, PTP Clear, Clear Controller, and Master Clear.

A necessary condition for this bit to be set is that the PTP be in START condition. PTP STOP will not reset this bit.

CP DATA (A11 = 1)

This status bit indicates, when set, that a Card Punch A/Q Data transfer operation may be performed.

Data Status becomes first set a few msec. after a CP Feed Request command, when the CP device is ready to accept data for first column punching.

The Data status bit is reset by reply to a Punch Data instruction and set again upon completion of data transfer to the device at each column punching.

The CP Data Status bit is cleared by CP Clear, CP Feed, Clear Controller, or Master Clear. When cleared, Data Status will become set again only after a new feed command.

NOTE:
Counting of the punched columns is not done by the Controller. This function is left entirely to the CPU. The end of a card should be determined by the CPU either by counting columns or by monitoring Status-1 bit CP-EOC.

On Bus (A12 = 1)

This bit will always be equal to "1". It corresponds to the status of the On Bus Flip-Flop (FF64), which is held constant at logical value "1" in order to enable the output of signals to the Card Punch device.

CP End of Card (EOC)

The EOC signal is the feed command acknowledgement and enable signal as generated by the device. It indicates the following information:

- transition from "1" to "0" indicating feed initialization by the CP device.
- EOC is set to "1" during step to column 80. This indicates that a data word exists to be punched in column 80. When last column punching is completed, CP Info Ready status bit becomes reset.

Controller Protected (A14 = 1)

This bit indicates that the PT/CP Controller is protected. In this state, only protected instructions are accepted, except status requests.

CP Ready (A15 = 1)

This status bit indicates that the CP Equipment is Ready and on-line. A Ready condition exists when there is a card in the Punch Ready Station, the CP Equipment power supply is in operation, the stacker is not full, there is no jam condition, and the interlock is closed. The bit becomes reset when any of the above conditions are not met. At the time that the CP device becomes Not-ready, the CP Data status bit, and the CP Info Ready and CP Feed signals are reset.

Paper Tape Reader Commands

Reject Conditions

All PTR commands are rejected when:

- Protect violation occurs (CPU output instructions only)
- Controller is Busy executing a Self-test or Clear Controller command.

PTR Start/Stop

This function is initiated by a Write signal with Q-bits coded as shown in Table 2-1.

Figure 2-4 shows the A-Register bit definition.

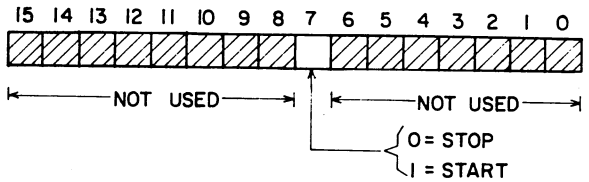


Fig.2-4. PTR START/STOP Definitions

The function is used to allow data transfer. A/Q data transfer is possible only when the START condition exists.

The STOP condition does not allow the data status bit to be set, but does not reset it, if set.

It should be noted that PTR Clear function resets the START condition (i.e. leaves the Controller in STOP condition).

PTR FORWARD/BACKWARD

This function is initiated by a WRITE signal with Q bits coded as shown in Table 2-1. This instruction specifies the direction for reading of the device. Figure 2-5 shows the A-Register Bit definitions.

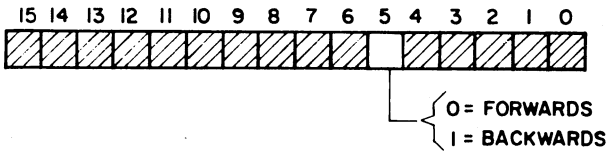


Fig.2-5. PTR Forwards/Backwards Bit Definitions

This function is accepted even if the PTR is Not-Ready. A bits A00 through A04 and A06 through A15 are not used (are ignored by the Controller).

This instruction directs the PTR to read in the backward direction when bit A05 is set, and in the forward direction when A05 is reset. Direction changes should only be performed when the Paper Tape Reader head is positioned in between the punched data blocks and when STOP mode exists.

The Controller continues in the same direction until a new PTR Forward/Backward Function is accepted. PTR Clear, Clear Controller, and MC set reading motion in the forward direction.

PTR Clear

This function is initiated by a WRITE signal with Q bits coded as shown in Table 2-1.

This instruction is the Clear Controller for the PTR logic in the Controller.

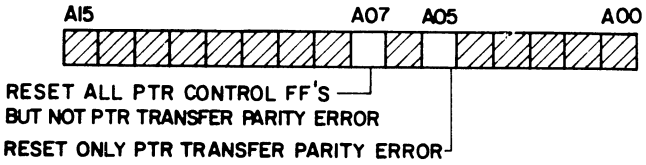


Fig.2-6. PTR Clear Bit Definitions

This function clears the PTR Data Status and the PTR control flip-flops, sets the reading motion in forward direction, and leaves the Controller in PTR STOP condition and in Character mode. Interrupt status request and response are not affected.

PTR Clear Interrupt

This function is the Clear Interrupt for the PTR logic in the Controller. It is initiated by a WRITE signal with Q bits coded as shown in Table 2-1.

A bits are not used (ignored by the Controller).

This function is accepted even if the PTR device is Not-Ready. This function clears the PTR Interrupt status requests and response.

PTR Interrupt Request

This function is initiated by WRITE signal with Q bits coded as shown in Table 2-1.

This function is accepted even if the PTR device is Not-Ready. A bits A00 through A04, A06 and A08 through A15 are not used (ignored by the Controller).

Figure 2-7 shows the A-Register bit definitions.

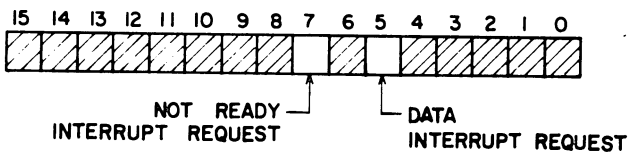


Fig. 2-7. PTR Interrupt Request A-Register Bits

Data Interrupt Request (A05 = 1)

This function sets the Data Interrupt Request bit for the PTR. It causes the interrupt response to be generated when data transfer may occur, i.e. data status bit is set. This bit is updated every time a PTR Interrupt Request command is issued.

The interrupt response is not cleared by reply to data transfer. The interrupt request and response are cleared by PTR Clear Interrupt, Clear Controller, and MC.

PTR Not-Ready Interrupt Request (A07 =1)

This function sets the Not-Ready Interrupt Request bit for the PTR. It causes an interrupt to be generated when the PTR Device Ready signal is false. This bit is updated every time a PTR Interrupt Request command is issued.

The interrupt request and response is cleared by PTR Clear Interrupt, by Clear Controller, or by MC.

Note that if a Not-Ready Interrupt is obtained and the PTR device becomes Ready, this interrupt still remains set.

PTR Data Mode (Character/Assembly)

This function is initiated by a Write signal with Q-bits coded as shown in Table 2-1.

This function is accepted even if the PTR device is Not-Ready. Figure 2-8 shows the A-Register bit definitions.

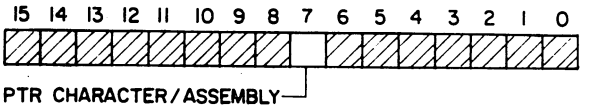


Fig.2-8. PTR Data Mode Bit Definitions

PTR Character/Assembly (A07)

When this bit is reset (character mode), the data character received from the device on lines D1 through D8 is transmitted to the CPU on A-Register lines A00 through A07 (where bit A00 corresponds to D1 etc.). Bits A08 through A15 are all zeroes.

When the bit A07 is set (Assembly mode), data transfer to CPU is 8 to 16 bit assembly. The first character received from the device is transmitted to CPU on A-Register lines A08 through A15 and the second character is transmitted on A-Register lines A00 through A07. The A/Q channel CHARINPUT line is not activated in either mode. PTR Character/Assembly mode should be determined when the PTR is in STOP mode. If START mode exists, the Controller rejects this command.

PTR Read Data

This function is initiated by a READ signal with Q-bits coded as shown in Table 2-1.

This function is accepted when the PTR data status bit is set. The data transfer depends on the Data Mode. When the Controller is in Character mode, the data character that is received from the device appears in A-Register bits A00 through A07, where bits A08 through A15 are zeroes.

When the Controller is in Assembly mode, the data consists of a 16 bit word where A-Register bits A08 through A15 contain the first character, and bits A00 through A07 contain the second character.

PTR Assembly Transfer Status

This function is initiated by a READ signal with Q-bits coded as shown in Table 2-1.

This function is accepted at any time. It is used to monitor data transfer status when assembly mode is selected. The status information is loaded into A-Register as shown in Figure 2-9.

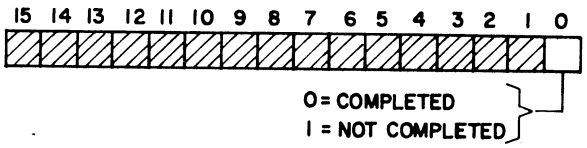


Fig.2-9. PTR Assembly Transfer Status

Bit A00 becomes reset when:

a) A 16-bit word has been transferred from the PTR device,
b) After PTR Clear, Clear Controller, and MC.

Bit A00 becomes set when only the 8 most significant bits of the 16-bit word have been transferred.

PTR Alarm Status

This function is initiated by a READ signal with Q bits coded as shown in Table 2-1

This function is accepted at any time.

This function is used to monitor parity errors when transferring data to the Controller.

The status information is loaded into A-Register as shown in Figure 2-10.

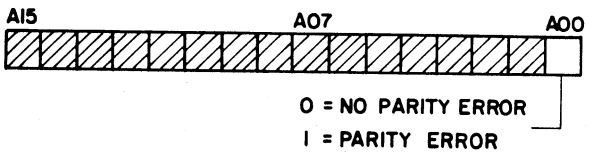


Fig.2-10. PTR Alarm Status, Bit Definitions

It should be noted that parity error bit remains set until a PTR Clear Command (A05 = 1) is issued.

PTR Operation

From the time that the Paper Tape Reader is connected and Ready and START condition exists, the PTR logic in the Controller moves between two states:

a) PTR Data Status reset - The Controller is in process of requesting and receiving a data character from device.
b) PTR Data Status set - The Controller contains a data character and is ready for AQ PTR Read-Data transfer operation.

PTR Data Status bit remains set until data transfer is completed. At that time, PTR Data Status is reset, and it becomes reset again when new data is received from the device.

Changes in operating parameters should be performed (preferably) when in the STOP mode.

Paper Tape Punch Commands

Reject Conditions

All PTP commands are rejected when:

- Protect violation occurs (CPU output instructions only)
- Controller is Busy
- Controller is in special test state.

PTP Start/Stop

This function is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1.

Figure 2-11 shows the A-Register bit definitions.

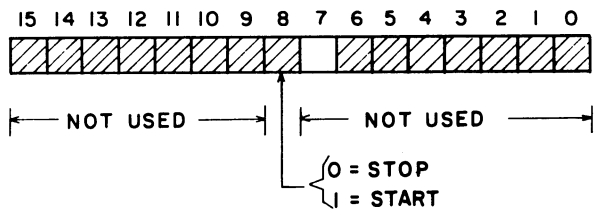


Fig. 2-11. PTP Start/Stop Bit Definitions

This function is used to allow data transfer. A/Q data transfer is possible only when the START condition exists.

The STOP condition does not allow the data status bit to be set, but does not reset it, if set.

Note that the PTP Clear function resets the START condition (i.e. leaves the Controller in the STOP condition).

PTP Device Function

This function is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1.

This function is accepted only when PTP Data Status bit is set.

Table 2-2 shows the A-Register bit definitions.

Note that the bits A08 through A15 are not used.

TABLE 2-2. PTP DEVICE FUNCTION BIT DEFINITIONS

A REGISTER								FUNCTION
7	6	5	4	3	2	1	0	
0	0	0	0	1	0	0	0	Back Stepping
0	0	0	1	0	0	0	1	Parity Error
0	0	0	1	0	0	1	0	Tape Low
0	0	0	1	0	1	0	0	Echo Error

The character specified by bits A00 through A07 is transmitted to the Paper Tape Punch device on interface lines D1 through D8 (where D1 corresponds to A00).

Back Stepping

Causes the PTP to backstep one character.

Parity Error

Questions the device if its internal parity error status is present. Device message status is set for positive answer and reset for negative answer. Parity error indicates a data transmission error between Controller and device.

Tape Low

Questions the device if its internal tape-low status is present. Device Message status bit is set for positive answer and reset for negative answer.

ECHO ERROR

Questions the device if its internal Echo-Error Status is present. Device Message status bit is set if answer is positive and reset for negative answer. The Echo-Error indicates wrong punching. The device internal statuses are related to the last punched character. They are updated after every new punched data character.

PTP Data

This function is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1.

This function is accepted when the PTP data status bit is set. The data transfer depends on the Data Mode. When the Controller is in Character mode, the data character is transferred to the Paper Tape Punch Device from A-Register bits A00 through A07, where bits A08 through A15 are ignored by the Controller. When the Controller is in Disassembly mode, the A-Register 16-bit word is transferred to the device as two 8-bit characters where the 8 upper bits are transferred first and the 8 lower bits are transferred last.

Figure 2-12 shows the A-Register bit definitions.

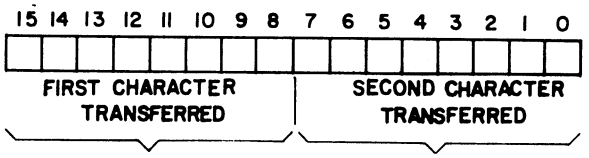


Fig.2-12. PTP Data A-Register, Bit Definitions (Disassembly Mode)

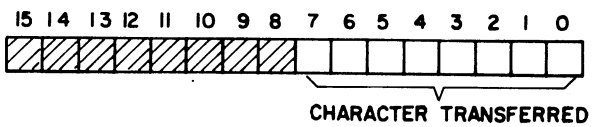


Fig. 2-13. PTP Data Bit Definitions (Character Mode)

PTP Clear

This function is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1.

This function is the Clear Controller for the PTP logic in the Controller. A-Register bits are not used (ignored by the Controller).

This function is accepted even if the PTP device is Not-Ready. It clears PTP-control flip-flops, Data Status bit, and leaves the Controller in STOP mode and Character mode (Interrupt status request and response are not affected by PTP Clear). It also clears the PTP CA FF and PTP Disassembly T, status FF.

PTP Clear Interrupt

This function is the Clear Interrupt for the PTP logic in the Controller. It is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1.

A-bits are not used (ignored by the Controller).

This function is accepted even if the PTP device is Not-Ready. This function clears the Interrupt Requests, Response, and Status.

PTP Interrupt Request

This function is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1.

This function is accepted even if the PTP device is Not-Ready. A-bits A00 through A04, A06, and A08 through A15 are not used (ignored by the Controller).

Figure 2-14 shows the A-Register bit definitions.

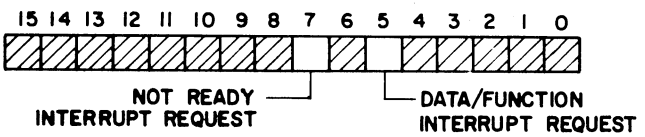


Fig.2-14. PTP Interrupt Request A-Register Bits

Data/Function Interrupt Request (A05 = 1)

This function sets the Data/Function Interrupt Request bit for the PTP. It causes an interrupt to be generated when a data transfer or Function code transfer may occur. This bit is updated every time a PTP Interrupt Request command is issued.

The Interrupt Response is not cleared by reply to data transfer or to function code transfer; therefore, a PTP Clear Interrupt command should be issued prior to every data or function transfer and a new request issued (if required) after the transfer.

The Data/Function Interrupt Request and Response are cleared by PTP Clear Interrupt, Clear Controller, or MC.

Not-Ready Interrupt Request (A07 = 1)

This function sets the Not-ready Interrupt Request bit for the PTP. It causes an Interrupt to be generated when the PTP device becomes Not-ready. This bit is updated every time a PTP Interrupt Request command is issued. The Interrupt Request and Response are cleared by PTP Clear Interrupt, Clear Controller, or MC. Note that if a Not-ready Interrupt is obtained and the PTP device becomes Ready, this interrupt still remains set.

PTP Data Mode (Character/Disassembly)

This function is initiated by a WRITE signal with Q-bits as shown in Table 2-1. This function is accepted even if the PTP device is Not-ready. A-bits A00 through A06 and A08 through A15 are not used (ignored by the Controller).

Figure 2-15 shows the A-Register bit definitions.

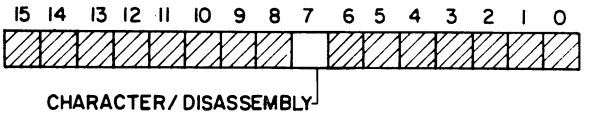


Fig.2-15. PTP Data Mode Bit Definitions

PTP Character/Disassembly (A07)

When this bit is reset (character mode) the data character is transferred to the PTP device from A-Register bits A00 through A07 where bits A08 through A15 are ignored by the Controller.

When this bit is set (disassembly) the A-Register 16-bit word is transferred to the device as two 8-bit characters where the 8 upper bits are transferred first and the 8 lower bits are transferred last. PTP Data Mode should be determined when the PTP is in STOP mode. If START mode exists, the Controller rejects this command.

PTP Disassembly Transfer Status

This function is initiated by a READ signal with Q-bits coded as shown in Table 2-1.

This function is accepted at any time. It is used to monitor data transfer status when disassembly data mode is selected. The status information is loaded into A-Register as shown in Figure 2-16.

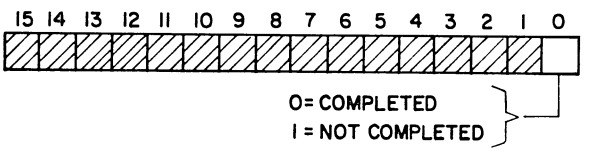


Fig.2-16. PTP Disassembly Transfer Status Bits

Bit A00 becomes reset when:

- A 16-bit word has been transferred to the PTP device,
- After PTP Clear, Clear Controller, and MC.

Bit A00 becomes set when:

-Only the 8 most significant bits of the 16- bit word have been transferred to the device.

PTP Operation

From the time that the Paper-Tape Punch device is connected and Ready and START conditions exist , the Controller moves between two states:

a) Data/Function Status set - the PTP logic in the Controller is ready to accept a data or Function Code Character for the device.
b) Data/Function Status reset - the PTP logic in the controller is in process of transferring a data or Function Code Character to the device .

Changes in operating parameters should be performed (preferably) when in the Stop mode.

If a PTP Clear is issued when the data/function bit is reset, and therefore when the Controller is in process of transmitting a character to the device, it may cause loss of that character without any indication of that occurrence to the CPU. Care should be taken when dealing with Device Message Status; it is valid (whether set or reset) only when data/function status bit is set.

Card Punch Commands

Reject Conditions

All CP commands are rejected when:

- Protect violation occurs (CPU output instructions only)
- Controller is busy
- Controller is in special test state.

CP Feed

This function is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1. This function is accepted when the CP device is in Punch Inhibit mode. A-Register bits are not used (ignored by the Controller). This function directs the CP to initiate a feed cycle, to advance the punched card to the Stacker, and to feed a new card from the Hopper through the Punch Ready Station to the punch station. The CP Feed instruction resets the CP data status bit. This bit is set again after Feed Acknowledge signal (CP EOC Status bit becomes reset). The CP Feed instruction should be issued only when the CP Data status bit is set to avoid feeding card before punching last character in present card. For full card punching , the CP Feed instruction has to be issued only after the EOC status becomes zero and the last data word for the last column (column 80) has been punched, (CP Info Ready Status bit reset), and when the Controller raises again the CP data status bit.

A CP Feed request issued while the controller is processing a card prevents further punching of data on the remaining columns of that card. When several columns are to be punched, CP Feed commands for the next card (if required) should be applied when data status is set. Error statuses of the current punched character should be checked when CP Data bit raises again.
It should be noted that in order to eject the last card to the stacker, there should be at least one additional card in the hopper since the Controller rejects any CP Feed command when the hopper is empty.

CP Clear

This function is the Clear Controller for the CP logic in the Controller. It is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1. A-register bits are not used (ignored by the Controller). This instruction is accepted even if the Card Punch device is Not Ready. This function clears the CP Data Status bit. Therefore, punching on the present card is no longer possible. This function also clears the Offset Command, Feed Command, and Info Ready

to device. Note that data to be punched can be ruined if a CP Clear command is issued while punching is performed. Therefore this command should be issued only when CP Data Status bit is set.

CP Clear Interrupt

This function is the CP Clear Interrupt instruction for the CP logic in the Controller. It is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1. A-register bits are not used (ignored by the controlller). This function is accepted even if the Card Punch device is not ready. This function clears the Interrupt Requests and Interrupt Response.

CP Interrupt Request

This function is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1. This function is accepted even if the Card Punch device is Not-Ready. A-register bits A00 through A04, A06, and A08 through A15 are not used (ignored by the controller). Figure 2-17 shows the A-Register bit definitions.

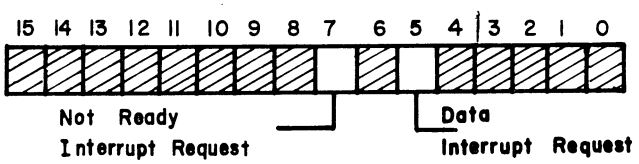


Figure 2-17: CP Interrupt Request A-Register Bits

CP Data Interrupt Request (A05 = 1)

This function causes an interrupt to be generated when data transfer may occur, i.e. when CP status is set. This bit is updated every time a CP Interrupt Request command is issued.

CP Data Interrupt Request is cleared by CP Clear Interrupt, by Clear Controller, and by MC. The Interrupt Response is not cleared after reply to data transfer; therefore a CPU CP Clear Interrupt command should be issued prior to every data transfer and a new request issued (if required) after the transfer.

CP Not-Ready Interrupt Request (A07 = 1)

This function sets the CP Not-Ready Interrupt Request bit. It causes an Interrupt to be generated when the Card Punch device is Not-Ready. This bit is updated every time a CP Interrupt Request command is issued. CP Not-Ready Interrupt Request is cleared by CP, Clear Interrupt, Clear Controller, and MC. Note that if a Not-Ready Interrupt is obtained and the CP device becomes Ready, this interrupt still remains set.

CP OFFSET

This function is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1. It is accepted even if the CP device is Not-Ready.

Figure 2-18 shows the A-Register bit definitions.

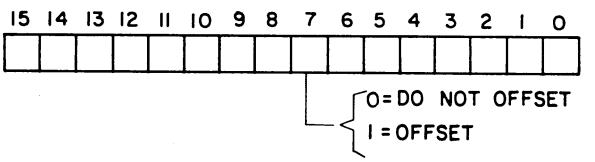


FIGURE 2-18 CP OFFSET, A-Register Bits

This function (when A07 = 1) directs the CP device to offset the card moving from the punch station to the stacker in response to a CP Feed command. The offset request refers to the card in process.

This bit is reset by the CP-Offset function with A07 = 0 by Clear Controlller or MC.

In order to offset one card, the following steps should be performed before the corresponding Feed is executed.

a) Issue a CP Offset A/Q command with bit

A07=1.
b) Issue a CP offset A/Q command with bit A07=0 (immediately after step 1).

CP DATA

This function is initiated by a WRITE signal with Q-bits coded as listed in Table 2-1.
A Data word of 12 bits is transmitted from the CPU via the Controller to the Card Punch device. This instruction is accepted when the CP Data status bit is set.
The CPU Data word is transmitted from A-Register A00 through A11, where the bits A12 through A15 are not used (ignored by the Controller). The bit-to-row correspondence is listed in Table 2-3.

Table 2-3. Correlation of A-Register Data Bits and Row Number

Row Number	A-Register Bits
Row 12 (top row)	A11
Row 11	A10
Row 0	A09
Row 1	A08
Row 2	A07
Row 3	A06
Row 4	A05
Row 5	A04
Row 6	A03
Row 7	A02
Row 8	A01
Row 9 (bottom row)	A00

CP Status 2

The CP Status 2 is initiated by a READ signal with Q-bits coded as shown in Table 2-1.

Figure 2-19 shows A-Register bit definitions.

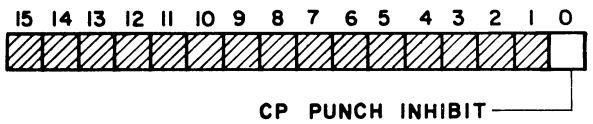


FIGURE 2-19: CP Status 2 A-Register Bit Definition

Bits A01 through A15 are not used (ignored by the Controller).

Note that no Alarm Condition will be generated if this error occurs;therefore, it is left for the CPU to check this status for each punched character.

CP Punch Inhibit (A00=1)

This status bit indicates that the CP device is in the Punch Inhibit mode, which means that Feed Requests and CP data instructions are not accepted by the Controller and device, and no punching occurs. This signal is controlled by a pushbutton located in the CP device.

CP Status 3

The CP Status 3 function is intiated by a READ signal with Q-bits coded as shown in Table 2-1.

Figure 2-20 shows A-Register bit definitions.

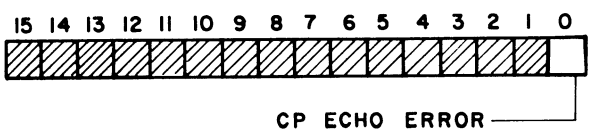


FIGURE 2-20: CP Status 3 A-Register Bit Definition

Bits A01 through A15 are not used (ignored by the Controller).

Note that no Alarm Condition will be generated if this error occurs; therefore, it is left for the CPU to check this status for each CP Echo Error (A00=1).
This bit indicates that a punch error in the CP device has occurred. (The Punch Echo-Check in the CP device does not agree with the requested punch data).
The CP Error status once set will be reset after the next Feed Cycle has been initiated.

CP Status 4

The CP Status 4 function is initiated by a READ signal with Q-bits coded as shown in Table 2-1.
Figure 2-21 shows the A-Register bit definitions.

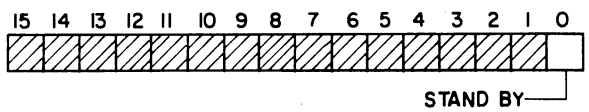


FIGURE 2-21: CP Status 4, A-Register Bit Definitions

Bits A01 through A15 are not used by the Controller.
Note that no Alarm Condition will be generated if this error occurs;therefore, it is left for CPU to check this status for each punched character.

Stand-by (A00=1)

This status bit indicates that the CP device is in Off-line mode.

CP Status 5

The CP Status 5 function is initiated by a READ signal with Q-bits coded as shown in Table 2-1.

Figure 2-22 shows the A-Register definitions.

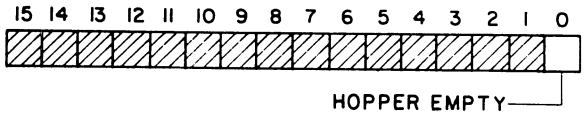


Figure 2-22: CP Status 5 A-Register Bit Definitions

Bits A01 through A15 are not used by the Controller.

Note that no Alarm Condition will be generated if this error occurs. Therefore it is left for the CPU to check this status.

Hopper Empty (A00=1)

This status bit indicates that the CP device input hopper is empty of cards.

Test- Type Commands

These commands are used to test Controller logic, registers, flip-flops, jump conditions, and data paths.

Upon receipt of any of these commands, the Controller becomes Busy, and the Busy Status -1 bit is set, remains set until test completion. When the Busy bit is set, all instructions are rejected by the Controller except Clear Controller and Status 1.
Any time one of the test-type A/Q instructions is issued (i.e. any CPU Out or Input instruction with Q3=1, Q4=0, and Q5=1), the Controller enters a special test state.

When in the test state, the Controller accepts only test-type A/Q instructions and rejects any other instructions except Clear Controller and Status 1.

Therefore, when in the test state, the Controller rejects operations which are related to the devices. To exit from the test state a Clear Controller command must be issued. At this time, all of the internal FF's of the three devices are reset. This command sets the necessary initial conditions for normal operations.

Self-Test 1

This function must be preceded by a Clear Controller. This function directs the Controller to check its internal data paths and ALU. The lower eight bits of the A-Register specify the data to be transferred along the internal paths of the Controller. The upper and lower eight bits of the A-Register specify the data which is to be operated on by the ALU.

Figure 2-23 illustrates the A-Register format.

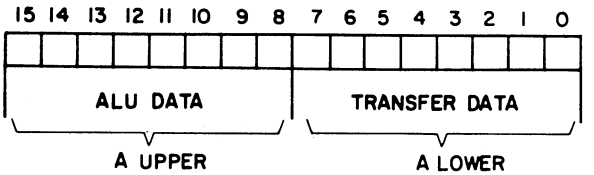


FIGURE 2-23 Selt-Test 1 A-Register Format

Upon acceptance of this command, the Controller becomes busy and remains busy until the internal transfers and ALU operations are completed. At this time busy status is reset. If busy bit is not reset within 2 msec., this indicates that the Controller is defective. After Busy status is reset, A-Out status should be read to determine the success of the test. The upper 8 bits of the A-Register should contain F_{16} plus the data that was originally sent in the lower eight bits of the A-Register in Self-Test 1. The lower eight bits should contain an expected result which is a function of the data originally sent in the upper and lower eight bits of the A-Register during Self-Test 1 according to the following equation:
A low=
((((Aup - 1) x 2 + $\overline{A}$ low) + 1 - Aup) A low) or Aup.
Figure 2-24 illustrates the Self-Test 1 result.

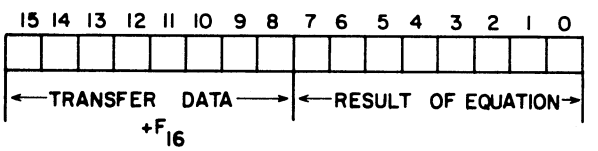


FIGURE 2-24: Self Test 1 Results

This instruction is rejected when the Controller is Busy. In Interrupt Response will be generated after Busy status becomes reset, if a Test Mode Interrupt Request command was issued prior to this function.
Self Test 1 will also load the 16 file registers in the following way:

FILE (0) = Transfer Data + F_{16}
FILE (1) = Transfer Data
FILE (2) = Transfer Data + 1
FILE (3) = Transfer Data + 2
FILE (4) = Transfer Data + 3
FILE (5) = Transfer Data + 4
FILE (6) = Transfer Data + 5
FILE (7) = Transfer Data + 6
FILE (8) = Transfer Data + 7
FILE (9) = Transfer Data + 8
FILE (A) = Transfer Data + 9
FILE (B) = Transfer Data + A_{16}
FILE (C) = Transfer Data + B_{16}
FILE (D) = Transfer Data + C_{16}
FILE (E) = Transfer Data + D_{16}
FILE (F) = Transfer Data + E_{16}

In general, $FILE_{(N)}$ will contain the transfer data plus (N-1), except $FILE_{(0)}$ which will contain transfer data plus F_{16}.

After reading A-Out status, the contents of the 16 file registers should also be read and examined for the proper data making use of Test Load File Address and Test Read File commands.

Self-Test 2

This function is initiated by a WRITE signal with the Q bits coded as shown in Table 2-1.

Self-Test 2 checks the Controller internal F/F's, jump conditions, and Status 1 F/F's. The A-register is not used for this command. Upon acceptance of this command, the Controller becomes busy until the test is complete. At this time Busy status is reset. If Busy bit is not reset after 2 msec., it indicates that the Controller is defective. For this function, an Interrupt Response will always be generated at the time that Busy status becomes reset. This bit is reset by a protected Clear Controller command, which should follow Self-Test 2. Prior to the execution of Self-Test 2, a Clear Controller command should be issued in order to ensure that all status 1 F/F's are in their quiescent state. Figures 2-25 and 2-26 illustrate Dynamic status after execution of Clear Controller and after execution of Self-Test 2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIGURE 2-25: Status 1 after Clear Controller

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0

FIGURE 2-26: Status 1 after Self-Test 2

When the test is complete (Busy status reset) A-Out status should be read directly following the completion of the test to determine if the test was successful. A-Out status $ACED_{16}$ indicates that the test was successful. A-Out status $DEAD_{16}$ or any other status indicates that the controller is defective.

If A-Out status gives the successful result ($ACED_{16}$) Status 1 should be read and compared to Figure 2-25. If these are not identical, the Controller is defective.

Self-Test 3

This function is initiated by a WRITE signal with Q bits coded as shown in Table 2-1. This function must be preceded by a Clear Controller command. This function directs the Controller to test the data paths interconnecting the Controller and PT Relay Sta-

tion. Receivers and Transmitters from the PT Relay Station to the devices are not tested.

A-Register bits (8 least significant bits) specify the data which is to be transferred along the PT Relay Station.
Figure 2-27 illustrates the A-Register format.

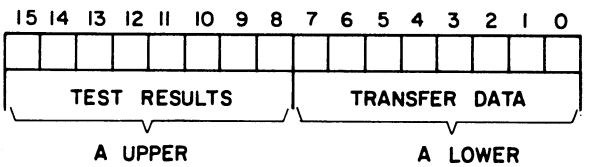


FIGURE 2-27: Self-Test 3, A-Register Bit Definitions

The test results will be available in the A-Out register (8 most significant bits) only after Bit Busy becomes reset. If the contents of the A-Out register do not equal the data sent,it indicates that the Controller or PT Relay Station is defective. This instruction is rejected when the Controller is Busy. An Interrupt Response will be generated after Busy status becomes reset, if a Test Mode Interrupt Request command was issued prior to this function.

Test Mode Load File Address

This function is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1.
This function is used together with Test Mode Read File command to allow CPU to check contents of File registers. This function is rejected when the Controller is Busy. Figure 2-28 shows A-Register bit definitions.

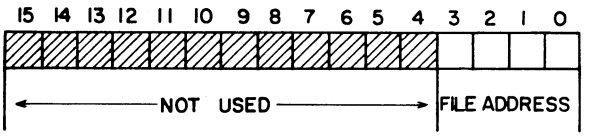


FIGURE 2-28 Test Load File Address, Bit Definitions

Test Mode Interrupt Request
This function is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1.

This function is used to generate an Interrupt Response at end of operation of Self-Test 1 and Self-Test 3.
This function is rejected when the Controller is Busy.

Test Mode Clear Interrupt

This function is initiated by a WRITE signal with Q-bits coded as shown in Table 2-1.
This function clears the Test Mode interrupt request and response.

A-Out Status for Self-Tests

This function is initiated by a Read signal with Q bits coded as shown in Table 2-1.
This function is used for reading the results of Self-Tests 1,2, and 3. After execution of one of these Self-Tests, the result will reside in the A-Out Register . Since this A-Out Register is also used for sending other data on the A-lines, self-test results should be read directly following the execution of the self- test to ensure the result.

Test Mode Read File

This function is initiated by a Read signal with Q bits coded as shown in Table 2-1.
This function is used together with Test

Mode Load File Address function in order to check the contents of the File Registers. Two consecutive file words are loaded into the A-Register. The lower eight bits will contain the contents of the file at the address specified by the Test Mode Load File Address command. The upper eight A-Register bits will contain the contents of the specified file address plus one.

INSTALLATION AND CHECKOUT

MANUAL CONTROLS

The following removable jumper plugs are located on the PC board of the PT/CP Controller.

Equipment Number Jumper Plugs (Q07 through Q10)

These four plugs are used to represent any number from 0 to F; they are used to assign an equipment number to the Controller. Any instruction sent by the computer must be accompanied by an equipment number (Q bits Q07 through Q10) that matches the setting of the plugs.

Controller Protector Jumper Plugs (UPO)

One common Protect jumper plug for all three devices. When inserted, only protected instructions (except status requests) are allowed access to the Controller.

Mode Jumper Plug (JM)

This jumper plug must be inserted for correct operation of the Controller. This jumper enables proper operation for special circuits in the Controller. The special circuits relate to the Card Punch device.

Maintenance Switches

ON/OFF Switch Operation

When in the "On-Line" position, enables normal Controller operation.

When in the "Off-Line" position, the Controller is disconnected from the Controller CPU bus and is placed in a maintenance mode. The type of "Off-Line" operation which is performed is a function of Maintenance Switches positions.

In the "Off-Line" mode, the Controller does not respond to any Computer requests (CPU internal reject).

Operation of Maintenance Switches

The type of "Off Line" operation that is performed is a function of switches MS1, MS2, and MS3. The following table shows the available "Off Line" operations. Switches MS1, MS2, and MS3 can be changed only when the ON/OFF Line switch is in the "On Line" position.

TABLE 3-1 Legal Jumper Plug Combinations

JUMPER NAME	FUNCTIONS
Q07 through Q10	Inserted as required to determine Equipment Number
UPO	IN - All devices protected OUT - Not protected
JM	Always In
ALD	Autoload Enable Not Used (in or out)
SB	Enable CP Ready Signal Always In
BP	Enable Optional Driver Signal Always Out
SD0 through SD3	Track Density Selection Jumpers (for CDD Contoller only) Not Used (in or out)
UP1 through UP3	Unit Protect Jumpers

TABLE 3-2 OFF-LINE OPERATIONS			
MS3	MS2	MS1	"Off-Line" Operation Performed
0	0	0	Not Used*
0	0	1	Not Used*
0	1	0	CP Triangular Data Pattern
0	1	1	CP All Ones
1	0	0	PTP Triangular Data Pattern
1	0	1	PTR Backward Motion
1	1	0	PTR Forward Motion
1	1	1	Not Used *

* If any of these combinations is selected, the Controller will wait until the "On-Line" mode is set.

The "Off-Line" operation will be performed if the corresponding device is "ready". On the contrary, if the specific device is "not-ready", the Controller will abort the "Off-Line" operation and will remain busy until the Controller is placed in the "On-Line" mode. Therefore, the device on which the maintenance is to be performed should be made "ready" prior to placing the "On/Off Line" switch in the "Off-Line" position. If the device becomes "not-ready" during the maintenance operation, the operation will be aborted. To re-start the operation when the device does become ready, the "On/Off Line" switch must be flipped to the "On-Line" position and then once more to the "Off-Line" position.

Placing the "On/Off -Line" switch in the "On-Line" position will terminate the maintenance operation.
The Controller performs automatically a Clear Controller command and normal operation can be continued.

Read Paper Tape Forwards
The Controller will read the paper tape in the forward direction until:
-the device becomes not-ready,
-"On-Line" mode.
All parity errors are gated off.

Read Paper Tape Backwards
The operation is the same as in Read Paper Tape Forwards except that the backward direction is used.

Punch Paper Tape, Triangular Data Pattern
The Controller will punch the paper tape with special data pattern until:
-the device becomes not-ready,
-acceptor message (AM=1)
-"On-Line" mode.
All parity errors are gated off.

Punch and Feed One Card, Triangular Data Pattern
The Controller will punch the card presently in the punch station with triangular data pattern until:
- end of card,
- device becomes not ready
- device punch inhibit,
- "On-Line" mode
If end of card is reached and the CP device is ready, this specific card will be fed to the stacker. All punch errors are gated off. It is assumed for this test that a card is present in the punch station.

Punch and Feed One Card, Data All Ones
This operation is the same a Triangular Data Pattern except that data all ones is used.

Cable Interconnections
Figure 2-1 shows the Controller-Devices configuration. The Controller to PT Relay Station cable is shielded twisted pair cable, 20 feet long. It runs directly from the computer backplane.

The PT Relay Station to Paper Tape Reader device cable is a single shielded cable, 5 feet long.

The PT Relay Station to Paper Tape Punch device cable is a single wire, shielded cable , 5 feet long.

The Controller to Card Punch device cable is a shielded twisted pair,cable, 15 feet long. It runs directly from the computer backplane.

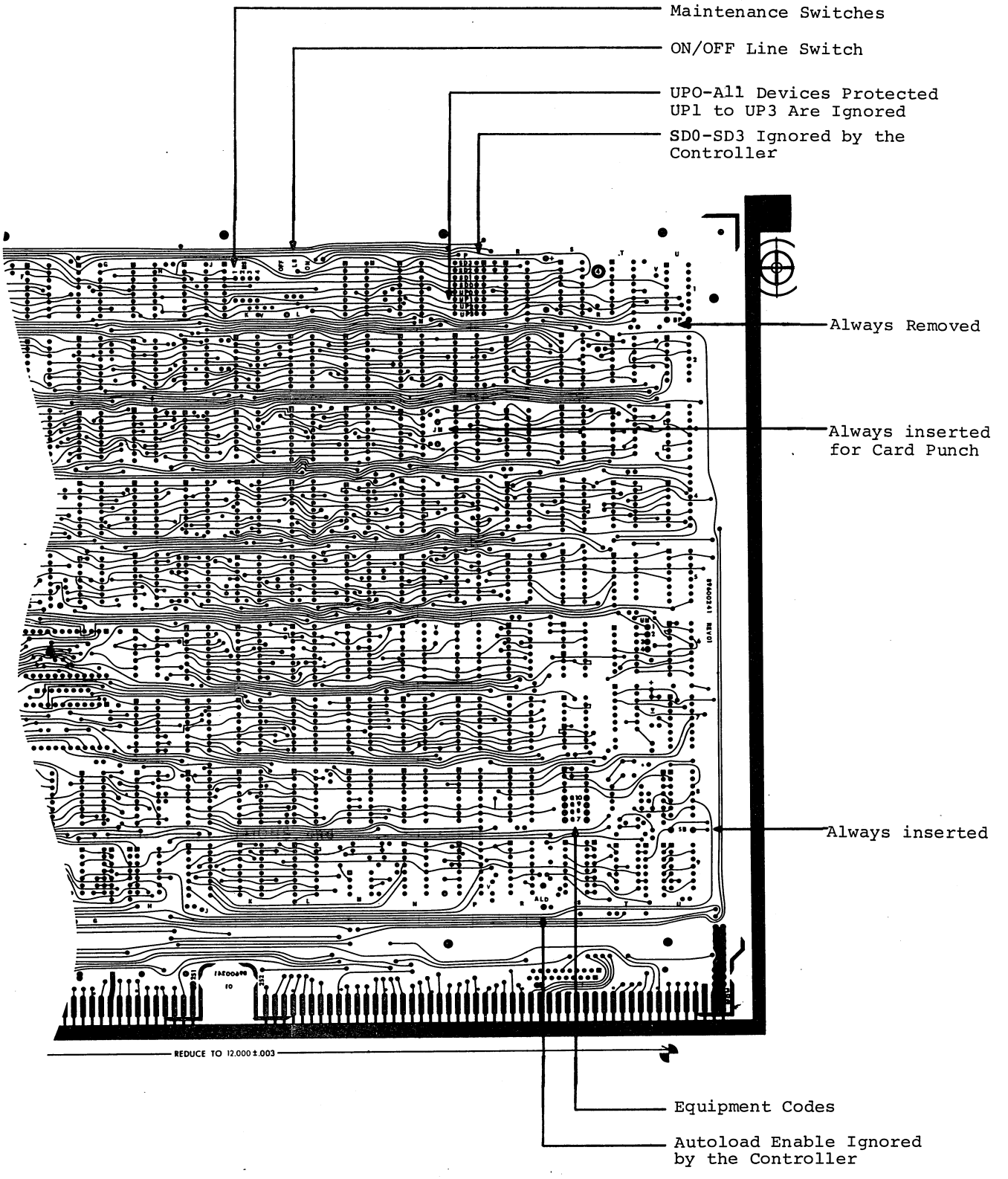


Figure 3-1. Jumper Locations on the PWB

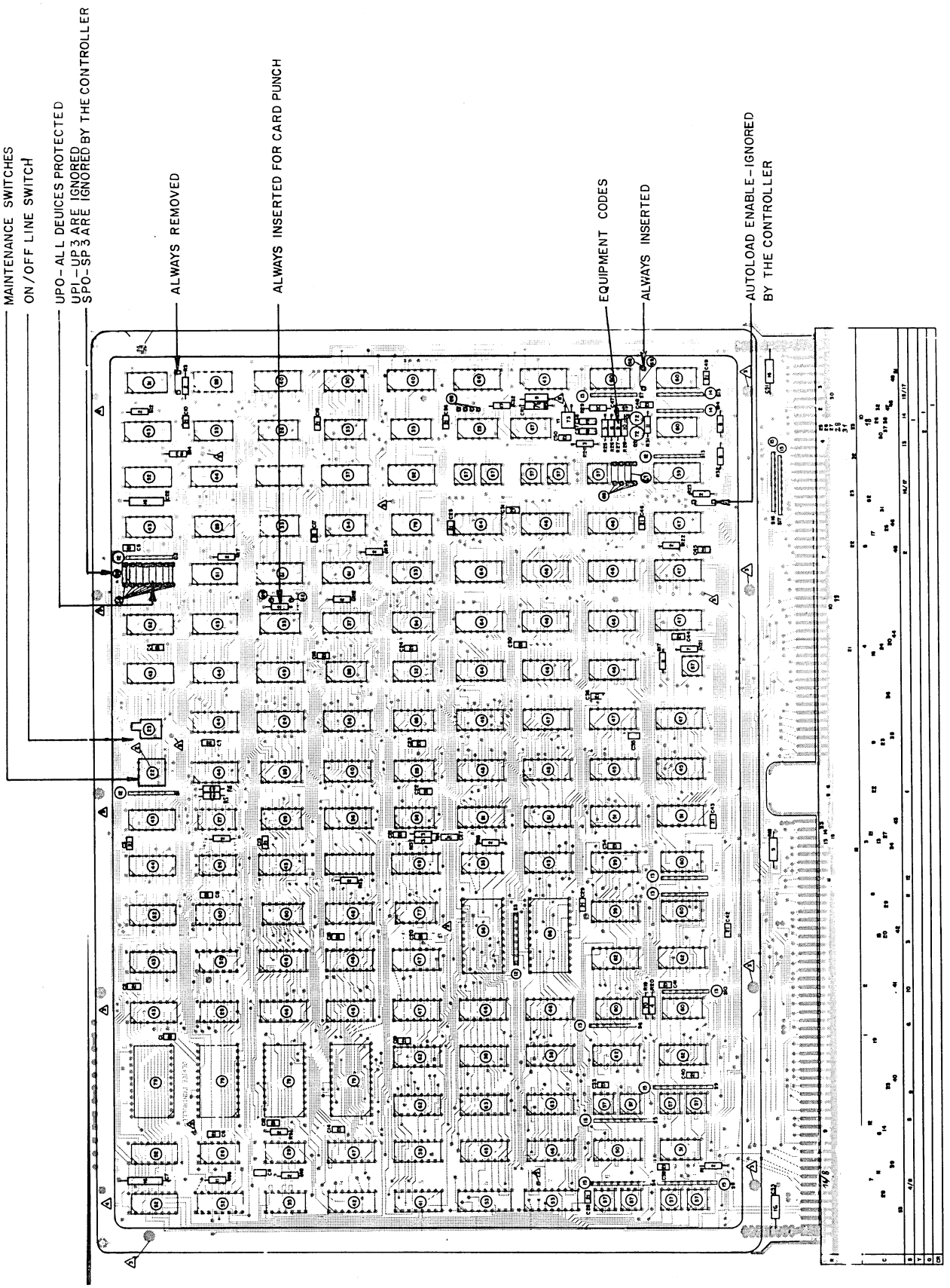


FIG 3-2 JUMPER LOCATIONS ON THE PWA

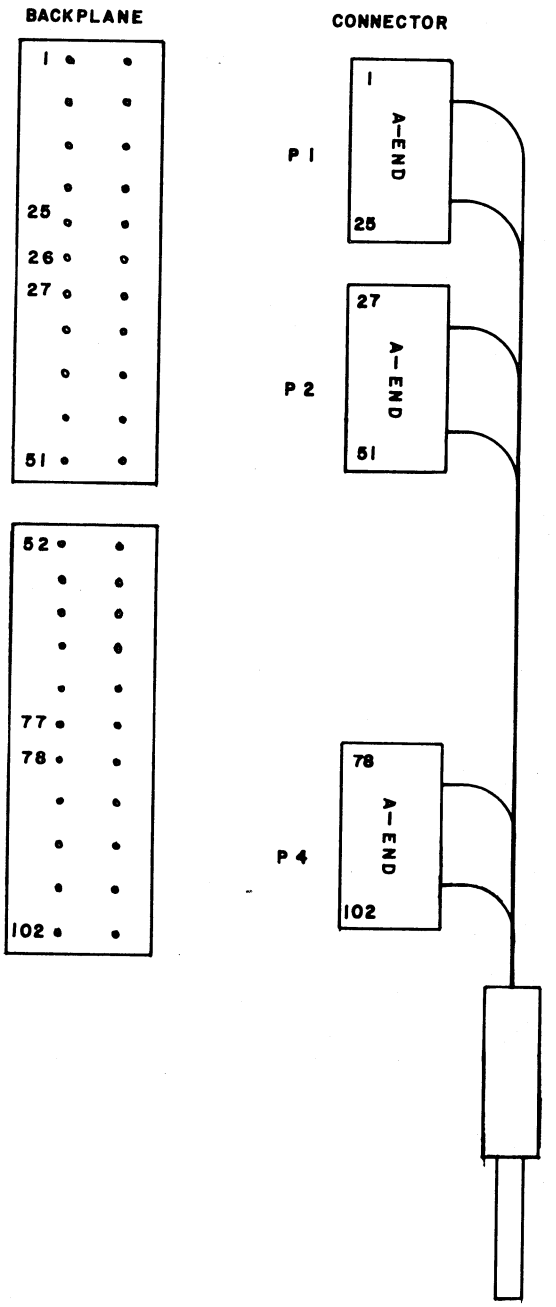


Figure 3-3. Cable Connection to Computer Backplane

THEORY OF OPERATION

Introduction

The Paper Tape Reader/Paper Tape Punch/Card Punch (PT/CP) controller provides the interface between the MP computer and the Facit 4020 Paper Tape Reader Facit 4070 Paper Tape Punch and CDC 9290 Card Punch devices.

The MP sends functions or states requests to the PT/CP controller via the A/Q channel. The functions received from the MP are decoded by the PT/CP controller. If the function requires the operation of any device, the controller will issue the appropriate command to the specific device. The PT/CP controller is a microprogrammed controller. The hardware is of a general nature with the firmware providing the means necessary to interface the three devices. The controller contains on one standard MP board a 1K x 16 bit PROM, an ALU performing logical and arithmetic operations, a 16 x 8 bit register file, auxiliary registers and other random logic necessary to read, decode and execute micro-instructions. Data transfers between the MP and the controller are made via the A/Q channel.

Interface, Controller and PT Devices

The Paper Tape Reader and Punch devices interface with the Controller via the PT Relay Station.

The Controller to Paper Tape devices interface signals conform to the rules of the Facit SP1 standard interface for parallel data transfer which provides for character-by-character transfer of data from a "source" to an "acceptor".

When interfacing with the Paper Tape Punch, the Controller performs the functions of the SP1-acceptor while the Paper Tape Reader device acts as the SP1-source.

Paper Tape Device Types

The Controller interfaces via the PT Relay Station with the following devices:

1) Facit-4020 Paper Tape Reader equipped with an SPI interface.

   The 4020 line of Readers are able to handle 5, 6, 7, or 8 track tapes at reading speeds of 0 to 300 characters per second.

   The 4020 line comprises the following model versions:

   a) Facit 4021 - Top-loaded table top version, with or without fan-folded tape handler.

   b) Facit 4022 - Front-loaded rack version, with or without fan-folded tape handler.

2) Facit - 4070 Paper Tape Punch equipped with Facit 5117/005 SP1 Interface, able to handle 5 and 8 track tape, or, alternatively, 6 and 7 track tape at punching speed of up to 75 rows per second.

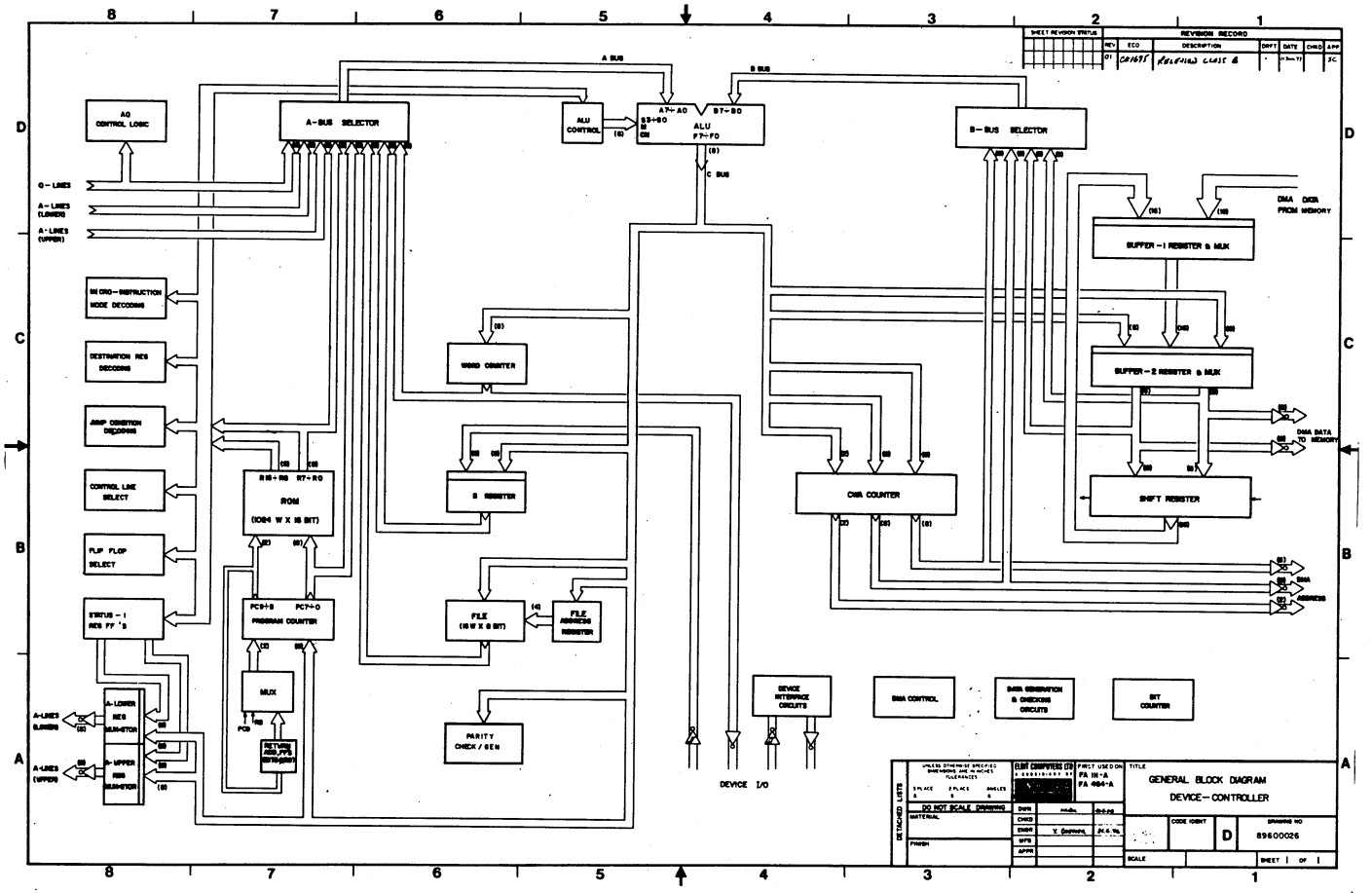


Figure 4-1. Common Device Controller Block Diagram

Signal Description

Z - Zero Voltage Reference

The zero voltage reference shall, in each device, be connected directly to the zero voltage point.

AO - Acceptor Operable

When the acceptor is operable it shall hold AO at "1".

When the acceptor is not operable, AO shall be "0".

In such a case, the other acceptor signals are undefined and can assume arbitrary levels. AC shall herewith be considered "0".

SO - Source Operable

When the Source is operable is shall hold SO at "1".

When the Source is not operable, SO shall be "0".

In such case, the other source signals are undefined and can assume arbitrary levels.

SC shall herewith be considered "0".

SO shall not depend on AO.

AC - Acceptor Control

The acceptor shall request information on the data wire by changing AC to "1" after -

a) it has ascertained that SC is "0";

b) it is ready to accept information on the data lines;

c) and AM is valid.

The acceptor shall accept the information on the data lines after it has ascertained that SC is "1". It shall then acknowledge the received information by changing AC to "0".

SC - Source Control

The source shall change SC to "1" after -

a) it has ascertained that AC is "1";

b) it has received AM; and

c) it has sent valid information to the data lines.

The source shall change SC to "0" after it has ascertained that AC is "0".

AM - Acceptor Message

At the same time that the acceptor requests new information on the data lines, it can transmit a message to the source using AM. The source shall keep AM at "0", if this signal is not utilized.

AM shall be valid before AC is changed to "1" and remain valid until the acceptor has ascertained that SC is "1".

CA - Control Available

Normally the source shall hold CA at "0". When special control status inform is transmitted using signals D1 through D8, the source shall hold CA at "1". The source shall hold CA at "0", if this signal is not utilized.

CA shall be valid before SC is changed to "1" and remain valid until the source has ascertained that AC is "0".

P - Parity

Odd parity bit is supplied and shall be transmitted using signal P. The number of "1's" in signal D1 through D8, CA and P shall thus add up to an odd number.

D1 through D8 - Data Lines

Data shall be transmitted using D1 through D8. D1 shall be used to transmit the least significant bit. Any signals, D1 through D8, that are not used shall be held at "0" by the source.

D1 through D8 shall be valid before SC is changed to "1" and remain valid until the source has ascertained that AC is "0".

Card Punch Signal Description

- Punch Data Row 1 to 12

  Data to device to be punched when Info. Ready signal is active.

- Read Command

  Initiates one card cycle. A Feed command may be sent to the device at any time.

- Status

  Indicates that motor turn-on has been completed. Goes to logic "0" one second after a Feed command. The absence of a Feed cycle within 15 seconds causes a return to logic "1".

- Busy

  Busy signal going to logic "1" indicates that the punch data has been transferred to the punch buffer.

- Offset

  Offsets a card in process. It must go to logic "0" prior to the initiation of a subsequent Feed cycle. Otherwise, it will refer to the next card.

- Info Ready

  This signal enables the signal column punch and wait feature of the device. Absence of this line will inhibit the punch cycle.

- Error

  Indicates error during punching. By Echo Check which is generated by a variable reluctance pick-up which is activated by a notch in the punch heads.

- End of Card (EOC)

  This signal is the Feed command acknowledge and enable signal. This line will go to a logic "0" on a Feed command and return to a logic "1" when the Feed command has been accepted by the device. In punch operation, EOC will go to a logic "0" during the step to column 80. EOC will return to a logic "1" at the next feed acknowledge.

- Punch Select

  This line selects Punch for On-Line operation.

- Punch Inhibit

  This line indicates when going to "0" that the punch cycle is inhibited.

- Ready

  Indicates that the Card Punch equipment is Ready and On-Line. Disabled by absence of card in Punch Ready Station, misfeed, jam, stacker full, motor circuit breaker.

- Stand-by (STBY)

  Indicates that the CP is Off-Line.

- Hopper Empty

  Indicates absence of cards in the Hopper.

CP Signal Timing

The interface signals timing is shown in Figure

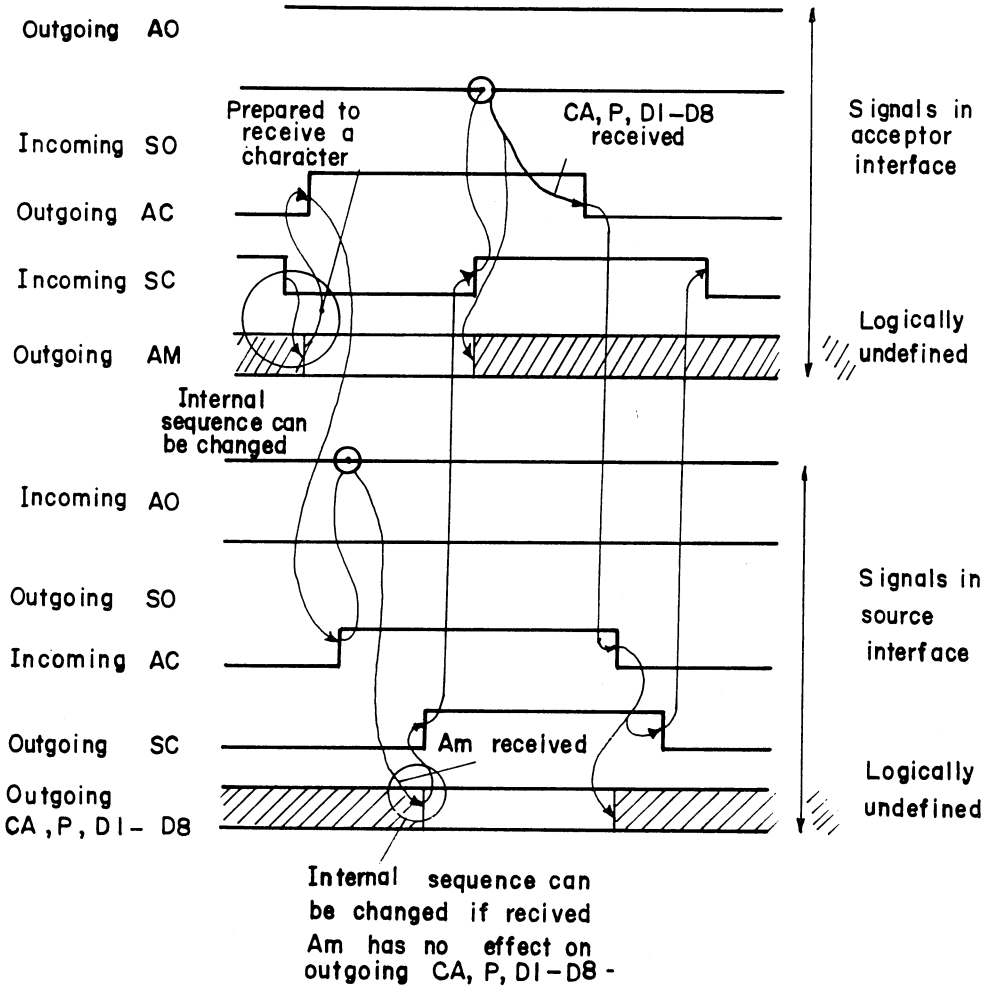
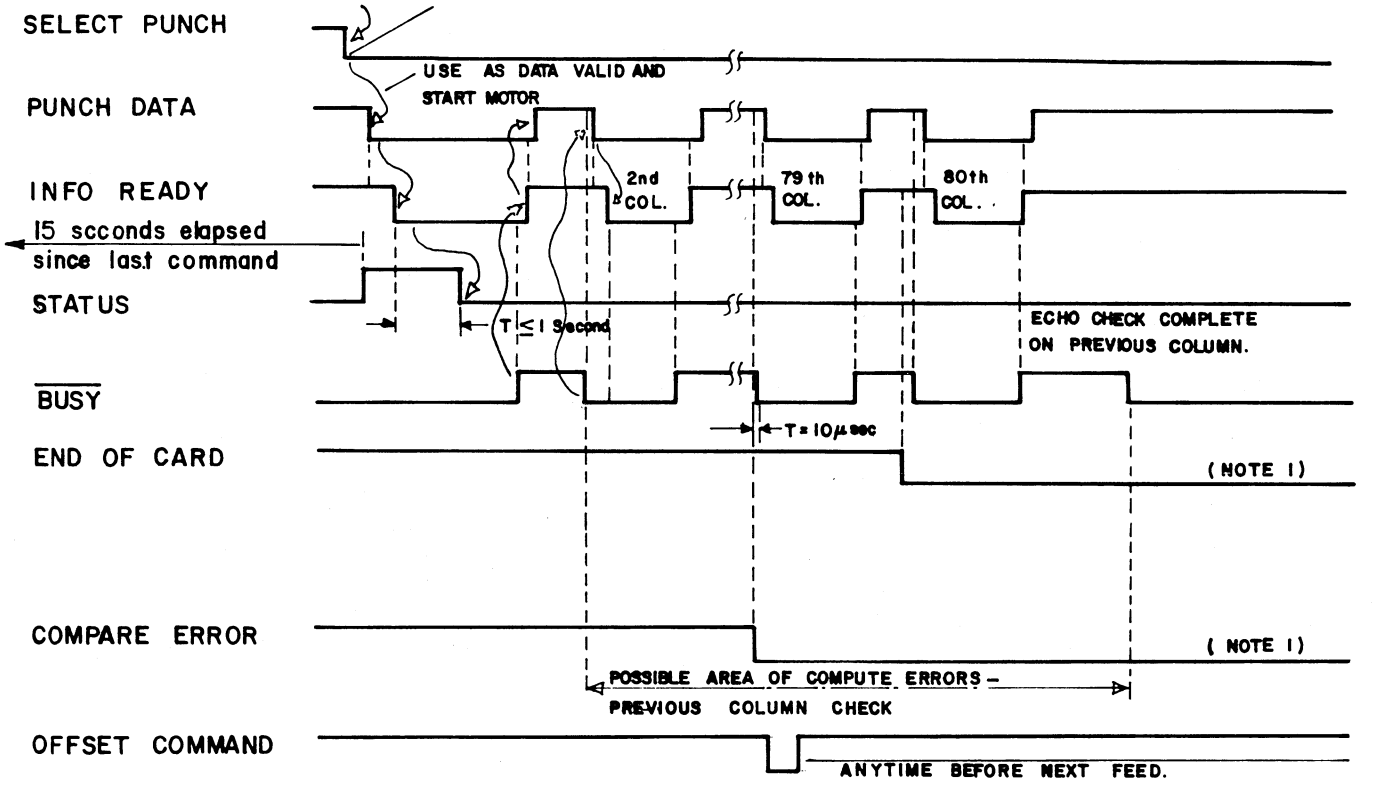


Figure 4-2. Interface Signals Timing



Above signals are the polarities as they appear on the I/O (I/O "TRUE" is logic "ZERO".)

NOTE 1. END OF CARD and COMPARE ERROR (if true) return to logic "ONE" after next FEED cycle has been initiated

Figure 4-3. Card Punch Timing Diagram

Initialization

Power on, master clear, or clear controller clears the program counter (PC). Upon completion of the MC or CC pulse, micro-code execution of the Clear Controller routine, whose starting address is zero, will commence. Three possible conditions can reset the PC to zero:

1) Master Clear (Power ON or from panel)
2) Clear Controller
3) Start and end points of any OFF-Line routine

Three types of routines are included in the micro-code:

1) A/Q command handling routines, regular and Test Mode
2) Internal controller, device handling routines
3) Off-Line maintenance routines

Once the clear controller routine has been executed, the controller enters a loop where all the internal controller device handling routines are sampled. This loop continuously samples the following jump conditions:

1) A/Q Execute FF set. This flip-flop will become set whenever an A/Q command with Q4=0 and the proper equipment code are received.
2) On/Off line switch. Whenever the off line maintenance switch is placed in the off line position this line will go low (active).

Whenever any one of the above conditions is active, an exit will be made from the loop and the required action will be performed.

Upon receipt of a test-mode command, the Controller becomes busy, the Busy Status-1 bit is set and remains set until test completion. The Controller also becomes busy for about 40 μsec (or less) upon receipt of a Clear Controller Command (the Busy bit is set for the duration). When the Busy bit is set all instructions are rejected by the Controller except Clear Controller and Status - 1.

Whenever one of the test-mode AQ instructions is issued (any CPU Output or Input instruction with Q3=1, Q4=0 and Q5=1), the Controller enters a special test-state.

When in the test-state the Controller accepts only test-mode AQ input or output instructions, except Clear-Controller and Status-1. Therefore when in the test-state, the Controller does not perform operations which are related to the device.

To exit from the test-state a Clear Controller command must be issued. This command sets the necessary initial conditions for normal operation.

A/Q Execute

The (Q bits) lines Q00-Q05 (Function code) together with the WRITE signal are one input to the A bus selector. When the A/Q Execute FF is detected as active by the micro-code, the Q input to the A bus selector is complemented, masked and loaded directly into the PC. This preload causes a 64 way micro program branch. Each of the 64 branch locations contains the starting address of the routine which performs the function whose code is found in Q00-Q05.

Not all 64 of the function codes are valid. The branch location of illegal codes contain a jump to the reject routine. This routine issues a reject and then jumps back to the loop.

Regular A/Q Command Handling Routines

These routines are checked for legality to determine whether they will be accepted (reply) or rejected. The conditions for reply or reject for each command are given in the Cyber 18 PT/CP Controller engineering specification.

The following is a description of the regular A/Q command handling routines:

PTR STOP/START - The lower 8 bits of the $\overline{A_L}$ are transferred to the B_{REG}. Most significant bit of the B_{REG} is tested; if equal to "1" PTR START MODE FF (RAM_{07}) is set, if equal to "0" PTR START MODE FF is reset. This function is used to allow data transfer. A/Q data transfer is possible only when PTR START condition exists.

PTR FORWARD/BACKWARD - PTR START mode condition is tested. If true (PTR START) the command is rejected. If false (PTR STOP) the lower 8 bits of the $\overline{A_L}$ are transferred to the B_{REG}. Bit 05 of the B_{REG} is tested; if equal to "1" PTRAM FF is set, if equal to "0" PTRAM FF is reset. This function directs the PTR to read in the forward direction if bit $B_{05} = 0$ and in backward direction if bit $B_{05} = 1$.

PTR DATA MODE - PTR START mode condition is tested. If true (PTR START) the command is rejected. If false (PTR STOP) the lower 8 bits of the A_L are transferred to the B_{REG}. Most significant bit of the B_{REG} is tested; if equal to "1" PTRAY FF is set, if equal to "0" PTRAY FF is reset. When bit B_{07} is reset (PTR Character Mode) the data character received from the device is transmitted to the CPU on A_{REG} lines A00 through A07. Bits A08 through A15 are all zeroes.

When bit B07 is set (PTR Assembly Mode) data transfer to CPU is 8 to 16 bit assembly. The first character received from the device is transmitted to the CPU on A_{REG} lines A08 through A15 and the second character is transmitted on A_{REG} lines A00 through A07.

PTR CLEAR - The lower 8 bits of the $\overline{A_L}$ are transferred to the B_{REG}. Bits B05 and B07 are tested; if B05 = 1 PTR PE FF (PTR Transfer Parity Error FF) is reset; if B07 = 1 all the PTR control flip-flops are reset (PTR PE FF is not updated).

PTR CLEAR INTERRUPT - PTR DIRQ (Data Interrupt Request), PTR NRDYIRQ (Not-Ready Interrupt Request) and PTR INT. FF's are reset. INTRSP FF is also reset if and only if PTP INT and CP INT FF's are reset.

PTR INTERRUPT REQUEST - The lower 8 bits of the $\overline{A_L}$ are transferred to the RAM_{04} location. In this way PTR DIRQ and PTR NRDYIRQ FF's are updated according to the values of bits A05 and A07.

PTR READ DATA - PTR DATA FF is checked. If reset, the function is rejected. If set, the contents of RAM_{09} is transferred to the $A\text{-}OUT_L$ and contents of $BF2_U$ is transferred to the $A\text{-}OUT_U$. Then PTRDTFF (PTR Data FF) is reset.

PTR ASSEMBLY TRANSFER STATUS - The contents of RAM_{08} is transferred to the B_{REG}. Most significant bit of B_{REG} is tested. If equal to "1", constant 01_{16} is loaded into $A\text{-}OUT_L$; if equal to "0", constant 00_{16} is loaded into $A\text{-}OUT_L$.

PTR ALARM STATUS - PTRPE (PTR Transfer Parity Error) condition is tested. If equal to "1", constant 01_{16} is loaded into $A\text{-}OUT_L$; if equal to "0", constant 00_{16} is loaded into $A\text{-}OUT_L$.

PTP STOP/START - The lower 8 bits of the $\overline{A_L}$ are transferred to the B_{REG}. Most significant bit of B_{REG} is tested; if equal to "1" PTP START MODE FF is set, if equal to "0" PTP START MODE FF is reset. This function is used to allow data transfer. A/Q data transfer is possible only when PTP START condition exists.

PTP DATA MODE - PTP START mode condition is tested. If true the command is rejected. If false the lower 8 bits of the $\overline{A_L}$ are transferred to the B_{REG}. Most significant bit of B_{REG} is tested; if equal to "1" PTPDY FF is set, if equal to "0" PTPDY FF is reset. When bit B07 is reset (PTP Character Mode) the data character is transferred to the PTP device from A_{REG} bits A00 through A07. Bits A08 through A15 are ignored by the Controller.

When bit B07 is set (PTP Disassembly Mode) the A_{REG} 16-bit word is transferred to the device as two 8-bit characters where the 8 upper bits are transferred first and the 8 lower bits are transferred last.

PTP CLEAR - All the PTP control flip-flops are reset.

PTP CLEAR INTERRUPT - PTP DIRQ (Data Interrupt Request), PTP NRDYIRQ (Not Ready Interrupt Request) and PTP INT FF's are reset. INTRSP FF is also reset if and only if PTRINT and CPINT FF's are reset.

PTP INTERRUPT REQUEST - The lower 8 bits of the $\overline{A_L}$ are transferred to the RAM_{05} location. In this way PTP DIRQ and PTP NRDYIRQ FF's are updated according to the values of bits A05 and A07.

PTP DATA - PTP DATA FF is checked. If reset, the function is rejected. If set, the contects of $\overline{AIN_U}$ are transferred to RAM_{OB}, and the contents of $\overline{AIN_L}$ are transferred to RAM_{OB}. Then PTPDT FF is reset and PTPIR FF (PTP Info Ready) is set.

PTP DEVICE FUNCTION - PTP DATA FF is checked. If reset, the function is rejected. If set, the contents of $\overline{AIN_L}$ are transferred to the WC_{REG}, PTPDT FF is reset, PTP CA FF and PTPIC FF (Index CA FF in RAM_{OA}) are set.

PTP DISASSEMBLY TRANSFER STATUS - PTPDS condition is tested. If equal to "1" constant 01_{16} is loaded into A-OUT_L; if equal to "0", constant 00_{16} is loaded into A-OUT_L.

CP FEED - Three conditions are checked: CPRDY (CP Ready), CPPUIH (CP Punch Inhibit) and CPHOEM (CP Hopper Empty). If the CP device is not-ready, and punch inhibit, or hopper empty conditions are true, the function is rejected. Otherwise control line CPFEST (CP Feed) is activated and CPDAT FF (CP Data FF) is reset.

CP CLEAR - All the CP control flip-flops are reset.

CP CLEAR INTERRUPT - CP DIRQ (Data Interrupt Request) CP NRDYIRQ (Not Ready Interrupt Request) and CP INT FF's are reset. INTRSP FF is also reset if and only if PTRINT and PTPINT FF's are reset.

CP INTERRUPT REQUEST - The lower 8 bits of the $\overline{A_L}$ are transferred to the RAM_{06} location. In this way CP DIRQ and CP NRDYIRQ FF's are updated according to the values of bits A05 and A07.

CP OFFSET - The lower 8 bits of the A_L are transferred to the B_{REG}. Bit B_{07} is tested; if B_{07}=1 CPOFFS FF is reset; if B_{07}=0 CPOFFS FF is set.

CP DATA - CP DATDAT FF (CP Data) is checked. If reset the function is rejected. If set, the contents of $\overline{AIN_L}$ are transferred to CWA_L and the contents of $\overline{AIN_U}$ are transferred to CWA_U. Then CPDAT FF is reset.

CP STATUS 2 - CP PUIH condition is tested. If true, constant 01_{16} is loaded into A-OUT_L; if false, constant 00_{16} is loaded into A-OUT_L.

CP STATUS 2 - CP ECER (CP Echo Error) condition is tested. If true, constant 01_{16} is loaded into A-OUT_L; if false, constant 00_{16} is loaded into A-OUT_L.

CP STATUS 4 - CP STBY condition is tested. If true, constant 01_{16} is loaded into A-OUT_L; if false, constant 00_{16} is loaded into A-OUT_L.

CP STATUS 5 - CP HOEM condition is tested. If true, constant 01_{16} is loaded into A-OUT_L; if false, constant 00_{16} is loaded into A-OUT_L.

Test Mode A/Q Command Handling Routines

The controller has three self tests for checking hardware via firmware.

Self Test 1 - checks the internal controller data paths and ALU operations. The data received from the CPU is divided into the upper and lower portions called A_U and A_L and transferred via the ALU to the B_{REG} and $BF2_L$ register. These registers feed the A and B side of the ALU, respectively. The logical/arithmetic operations specified by the self test 1 equation are performed on these two register and the result is placed in the lower portion of the A-OUT register. The A_L data is then transferred and incremented through all sixteen file registers and then through all the controller registers with the A-OUT_U being the final destination of the data. The CPU can examine the Self Test 1 result (contained in the A-OUT register) by reading A-Out status.

Self Test 2 - checks FF's and jump conditions. Every FF connected to a jump condition and concerning the PTR, PTP and CP operation is first reset and checked. Any active FF will cause the Hex. value DEAD to be placed in the A-OUT register. After testing for the reset condition the FF's are set and then tested for the set condition. CP FF's activated by control lines are also tested both in their set and reset states. If all tested conditions are in the proper state, the program will load $ACED_{16}$ into the A-OUT register.

Self Test 3 - checks data paths interconnecting the controller and the PT-Relay Station. The lower 8 bits of the $\overline{AIN_L}$ are loaded into WC_{REG} (like data to be punched) and return back to AIN_U via B_{REG} (like read data). The CPU can check that $A\text{-}OUT_U$ equals $A\text{-}OUT_L$ by reading A-OUT status. Control signals for the PTR and PTP devices are also checked using the corresponding FF's and jump conditions. Any error will cause value $1428_{16}/8241_{16}$ to be placed in the A-OUT register.

Test Mode Load Ram Address - The lower 8 bits of $\overline{AIN_L}$ are loaded into the Ram Address register and also into the B_{REG}. Then the contents of $B_{REG}+1$ is loaded into $BF2_L$ (value to be used in test mode Read RAM command).

Test Mode Interrupt Request - This function simply sets PTRPE FF (to be used as an index FF in special loop for test mode commands).

Test Mode Clear Interrupt - This function resets PTRPE and INTRSP FF's.

Test Mode A-Out Status - This function simply issues a reply sending the contents of the controller A-Out register to the CPU.

Test Mode Read RAM - Two consecutive RAM words are loaded into the A-OUT register. $A\text{-}OUT_L$ contains the contents of the RAM at the address specified by the Test Mode Load RAM address command. $A\text{-}OUT_U$ contains the contents of the specified RAM address plus one ($BF2_L$).

Internal Controller Device Handling Routines

Common Interrupt - This program controls the interrupt response line (INTRSP FF). PTRINT, PTPINT and CPINT FF's are checked. If all of them are reset, INTRSP FF is reset; otherwise INTRSP FF is set.

Set PTR AC Signal - This program activates the PTR AC signal. The conditions checked are: PTR AC FF reset, PTRDT FF reset, PTR start condition, PTR SO signal active, and PTR SC signal inactive. If any of these conditions is not true, signal PTR AC remains inactive (PTR AC FF is reset).

PTR Character Transfer - This program loads the B_{REG} with an 8 bit character read from the PTR device. The conditions checked are: PTRBF FF (B Register full) reset, PTRAC FF set and PTRSC signal active. Parity bit for this character is also checked and in case of error, PTRPE FF is set. At the end of this program PTRBF FF is set.

PTR Character Handling - This program acknowledges the receipt of data by resetting PTRAC FF. The conditions checked are: PTRBF FF set and PTR start condition.

PTRAY FF is also checked; If PTRBF FF is reset then constant 00_{16} is loaded into $BF2_U$; if FF PTRBF is set then PTRAY FF is checked and if found reset, the contents of RAM_{09} are loaded into $BF2_U$. If PTRPE FF is found set, the contents of $BF2_U$ are not changed.

PTR Interrupt - This program sets INTRSP FF in the following conditions:

1) PTR SO signal inactive and PTRNRDYIRQ FF (RAM_{04} bit 07) set;
2) PTRDT FF set and PTR DIRQ FF (RAM_{04} bit 05) set.

Set PTP Data/Function Status - This program sets PTPDT FF if the following conditions are met: PTP Start condition, PTP AC signal active, PTPSC FF reset, PTPIR and PTP Index CA FF's reset. If PTPAM signals found active, PTPDT FF is set without checking PTPIR and PTP Index CA FF's. If working in disassembly mode (i.e., PTPDY FF set) and FF PTPSC is found to be set, PTPDT FF is not updated.

Set PTP SC Signal - This program sets PTPSC FF if the following conditions are met: PTP Start condition, PTPAC being active and PTPSC FF being reset. The contents of RAM_{OA} (character to be punched) if transferred to the WC_{REG}. Status of the PTPDT FF is also checked. PTP PAR FF is updated according to the value of PTR LTC signal.

PTP Interrupt - This program sets INTRSP FF in the following conditions:

1) PTP AO signal inactive and PTPNRDY IRQ FF set;
2) PTPDTFF set and PTPDIRQ FF set.

Set CP Data Status - This program sets CPDAT FF if the following conditions are met: CPRDY signal being active, CPPUIH, CPINF, CPFED and CPBSY signals being inactive.

CP Interrupt - This program sets INTRSP FF in the following conditions:

1) CPRDY signal inactive and CPNRDYIRQ FF set;
2) CPDT FF set and CPDIRQ FF set.

PTR Ready Status - This program resets the PTR control FF's if signal PTRSO is inactive.

PTP Ready Status - This program resets the PTP control FF's if signal PTPAO is inactive.

CP Ready Status - This program resets the CP control FF's if signal CPRDY is inactive.

Off-Line Maintenance

All of the Off-Line Maintenance operations are initiated by the detection of an active signal caused by the ON/OFF Line switch being in the OFF position. An exit is made from the normal loop to a routine generating a delay of about one second. Maintenance switches 1, 2 and 3 are decoded and the selected operation is performed. Each of the operations continuously samples the ON/OFF Line switch. The Clear Controller routine is executed before and after any maintenance routine.

LOGIC DESCRIPTION

A/Q INTERFACE

INPUT-OUTPUT OPERATIONS

The necessary conditions for an A/Q Input or Output operation are as follows:

1. The equipment code msut match the equipment number.
2. The W=0 field signal $\overline{\text{WEO}}$ must be active.
3. The Read or Write signal, as required, must be active.

Equipment Identification

The equipment number is determined by four jumper plugs individually inserted into (or removed from) socket terminals marked Q7, Q8, Q9, and Q10 at location S8B. Inserting s jumper plug onto the Q7 terminal, for example, selects a "1" for that bit. Removing a jumper plug from the Q8 terminal selects a "0" for that bit, and so on. The four hexidecimal bits of the equipment code are received form the computer on the $\overline{\text{ADR 8}}$, $\overline{\text{ADR 9}}$, $\overline{\text{ADR 10}}$ and $\overline{\text{ADR 11}}$ lines at pins 281, 282, 283, and 284 respectively. These four signals are compared with the equipment code jumper settings.

Comparison of Equipment Number and Code

The equipment code bits from the computer are compared to the equipment number jumper plug settings by a 4-bit magnitude comparator at S9. If the compared bits match and the $\overline{\text{WEO}}$ signal is low, (i.e. "A=B in" (S9-3) is high) the "A=B out" comparator output (S9-6) will go high. The high output obtained at S9-6 is the first condition necessary for activation of the A/Q Interface Sequencer (high level at U4-1).

The W Field

The signal $\overline{\text{WEO}}$ must be low for Read or Write operations. If the W field=0 condition exists, then $\overline{\text{WEO}}$ at pin 292 will be low. This signal is received and inverted to a high level by a Schmitt-Trigger inverter T9-11/10; T9-10 is connected to Comparator "A=B in" input (S9-3).

The READ Signal

The third condition for a Read operation is an active (low) $\overline{\text{READ}}$ signal from the computer at pin 248 ($\overline{\text{READ SSTB}}$). If READ is active then $\overline{\text{READ}}$ at H9-13 will be low, and the inverter output (READ BUF) will be high at H9-12. The signal READ BUF is connected to: the flip-flop "Data In" at T4-12, a "2 input positive-OR gate" at T5-9 and the A-Bus Selector at F8-6.

When READ BUF is high, the output of the OR gate at T5-8 will be high. This provides the second enable to the 3-input positive NAND gate at U4-2.

The WRITE Signal

The third condition for a Write operation is an active (low) $\overline{\text{WRITE}}$ signal from the computer at pin 290. If WRITE signal is active, then T9-3 will be low and the output of this inverter at T9-4 will be high. This output (T9-4) is connected to: an OR gate at T5-10, a three input positive AND gate at U4-10 and a a positive two input NAND gate at R2-9.
For a Write operation, the output of the OR gate at T5-8 goes high and gives the second enable at U4-2.

SEQUENCER Enable

If the On-Off LINE switch (location L1) is in the "ON" position the Sequencer at location U3 is able to initiate a sequence of pulses. The enable is affected by release of the clear input at U3-1.

The hardware uses a digital filter formed by two flip-flops of the Hex D type at location U6. When U4-12 goes high, the OR gate output (T5-11) will also go high. U4-12 is connected to U6-4; U6-5 will go high after 0 to 50 nanosec (the clock of U6 is 20 MHz). U6-5 is connected to U6-14; U6-15 will go high after an additional 50 nanoseconds. The result is that the signal at T5-13 will go high 50 to 100 nanoseconds after the leading edge of U4-12.

POWER-ON Reset

This circuit generates a reset pulse at Power-On. C32 is charged through R30; at this time the inputs T7-2 and U6-1 are low. NOTE: The UM1, UM2, UM3, and UM4 are external connection points.

The diode D1 is used to discharge the capacitor at Power-Off.

The $\overline{\text{Master Reset}}$ signal from pin 46 is received at G9-13 (Schmitt Trigger Inverter). The flip-flops U6-3/2 and U6-13/12 form a digital filter. When G9-12 is high, U6-3 and T6-5 will also be high. U6-2 will go high after approximately 50 nsecs, raising U6-13 to a high level. U6-12 will go high after an additional 50 nsecs. If the $\overline{\text{MR}}$ signal at G9-13 is still active after the delay of 100 nsecs, T6-6 will go low driving T7-3 low which will in turn generate a low level at T7-6. The $\overline{\text{GR}}$ signal (fromT7-6) will drive U1-3 high generating the master reset pulse.

CLOCK Circuit

The controller incorporates a 20 MHz X-TAL oscillator. The oscillator is built from Q1 and Q2 transistors, T7-9,10/8; T6-13,12/11 and T6-9,10/8 gates, Y1 crystal, capacitors and resistors. The output is a 50 nsec pulse with a duty cycle of 50 percent.

Phase Generator

The 20 MHz is the clock input at U6-9. The flip-flop U6-6/7 and the NAND gate T6-1,2/3 form the 20 MHz divider. The output is a 10 MHz clock.

U5 is a Hex D-type flip-flop. The connections U5-5 to U5-6 and U5-7 through T3-13/12 to U5-4 form the first part of a phase generator. G2 is a Decoder/Demultiplexer. The inputs 1A (G2-2) and 1B (G2-3) are connected to U5-5 and U5-7; G2-4, 5, 7 and 6 are the phase generator outputs $\overline{\emptyset 0}$, $\overline{\emptyset 1}$, $\overline{\emptyset 2}$, and $\overline{\emptyset 3}$ respectively

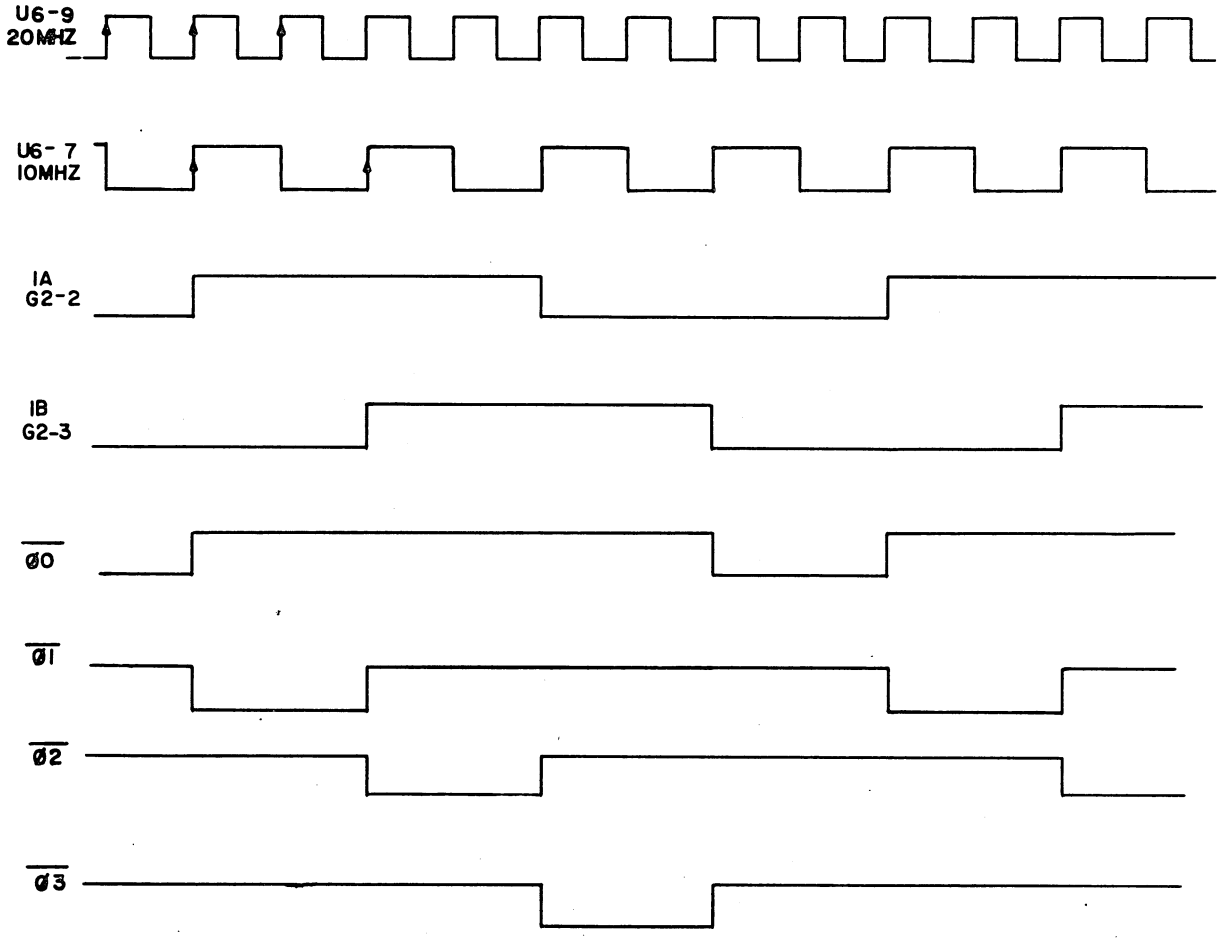


Figure 5-1. Phase - Generator Pulses.

Note: Phase pulses $\overline{\phi 0}$, $\overline{\phi 1}$, $\overline{\phi 2}$ and $\overline{\phi 3}$ have a pulse-width of 100 nsec each.

Sequencer

Flip-flop U3 is the sequencer used for A/Q commands.

The sequencer is clocked at 10 MHz.

When the controller receives an A/Q command (in the ON LINE state), the sequencer input U3-1 (clear) goes high.

The leading edge of the first 10 MHz clock pulse (U3-9) initiates the sequencer operation.

When an immediate reject condition exists, the Controller generates the Reject signal at S0 (U3-10) and the Sequencer stops (Q low level at U2-10 AND gate determines low at U3-14 Data Input).

If an immediate reject condition does not exist, S0 causes the generation of S1 (U3-15).

Pulse S2 is generated when the A/Q command is a Clear Controller or a Read Dynamic Status command. For Clear Controller or Dynamic Status commands, $\overline{\text{ADR 5}}$ is low (thus making Q4 equal to 1). AND gate input U2-13 is high, and Data Input U3-13 (S1·Q4) is high.

If S1·Q4 is high, the sequencer generates pulses S2 and S3. The leading edge of pulse S3 generates the Reply pulse.

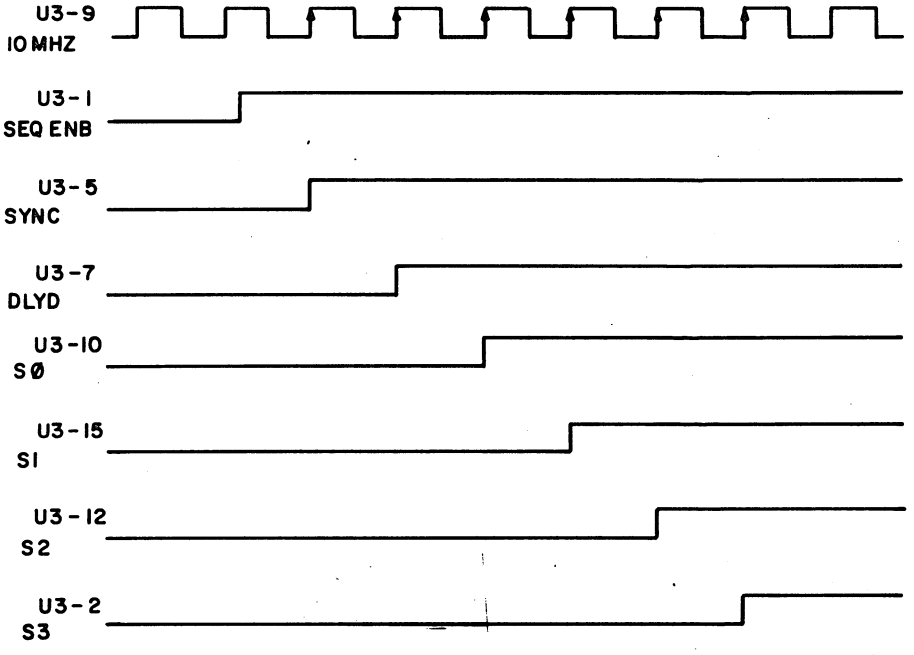


Figure 5-2. Sequencer Outputs

Reject Circuit

The A/Q commands with Q4=0 ($\overline{ADR\ 5}$ = high) cause a reject condition if the controller is in the busy state. In this case, flip-flop BUSY (G1-5) is high, U2-5 is high, U2-4 is high, and AND gate output U2-6 is high. The flip-flop U6-11/10 and the AND gate U2-1,2/3 form a digital filter for the Q4 line.

Another condition for Reject is protect violation. If flip-flop CNTPRT (B1-12) is high , the controller is protected. An unprotected A/Q Write command causes a protect violation (U4-8 is high). Flip-flop T4-2,3/5 is the Reject FF. A Reject condition (T4-2 high) causes the generation of the Reject pulse at the leading edge of S0.

If the A/Q command requires micro-program intervention, the program determines if and when the controller will send a Reject pulse to the CPU. In this case the control line $\overline{REJ}$ sets the Reject flip-flop (active low signal at T4-4). The reject pulse is transmitted to the CPU via driver B9-13,12/11, to pin 220.

Reply Circuit

Flip-flop T4-12,11/9 is the Reply FF. For A/Q commands with Q4=1, reply condition (T4-12 high) causes generation of the Reply pulse at the loading edge of S3.

If the A/Q command requires micro-program intervention, the program decides if and when the controller will generate a Reply pulse. In this case, the control line $\overline{RPLY}$ sets the Reply flip-flop (active low signal at T4-10).

The Reply pulse is transmitted through driver B9-9,10/8 to pin 218. The Reply and Reject circuits are enabled only at the time of an A/Q command (T4-13, and T4-1 are both high).

Micro-Program Execute Circuit

All A/Q commands with Q4=0 require micro-program intervention.

Flip-flop T2-12,11/9 is the micro-program execute FF. The leading edge of S1 sets the flip-flop when T2-12 is high (Q4=0).

The Clear Controller A/Q command (Q4=1) sets the RMEXEC flip-flop by an active low pulse at T2-10.

$\overline{REJ}$, $\overline{RPLY}$ or $\overline{GR}$ pulse reset the RMEXEC FF (T1-13 will be low through AND gate U4-3,4, 5/6).

RMEXEC is connected as a Jump Condition (T1-14).

Controller Reset

The controller is reset by a $\overline{GR}$ pulse (T7-6) or by a Clear Controller A/Q command (Q4=1).

The Clear Controller generates an active low pulse at R2-8 (NAND gate). This pulse, like the $\overline{GR}$ pulse generates a CCMR1 active high pulse at U1-3 driver output and a $\overline{CCMR2}$ and $\overline{CCMR3}$ active low pulse at J2-10 and J2-12 driver outputs.

A Clear Controller or $\overline{GR}$ pulse clears the Program Counter and activates the program from the first PROM address (000_{16}).

A-Output Register

The Multiplexers with Latched Outputs at F4,E3, E4, and F3 form the A-Output Register. F4 and E3 store the eight least significant bits, and E4 together with F3 store the most significant bits of the controller A-channel outputs. The ALU output bus is multiplexed with the Dynamic Status FF's at the input to the A-out register.

When a dynamic status request is received by the controller, Q4 is high and the read signal will be active; S1·Q4 is high and the multiplexers select the Dynamic Status bits (F4-10, E3-10, E4-10, and F3-10 will be high) as the input to the A-Out register.

The exclusive OR gate (R4-1, 2/3) generates the SPLS pulse. This pulse is transmitted through E2-9,10/8 and E2-12,13/11 NAND gates to clock the outputs of the Dynamic Status FF's into the A-Out register on the trailing edge of the SPLS pulse.

Under program control the clock for the A-Out upper and A-Out lower registers is generated by the destination decoder (K2-11 and K2-14 respectively) whenever the A-Out registers are slected as the destination registers by the micro-program.

A-Out Register Buffer

The A-Out register outputs are driven by inverting tri-state buffers at locations E5, F5, and B4. The buffers are enabled by output of the NAND gate at B3-6 which places the A-Out register contents on the A-channel during A/Q read commands.

A-Bus Selector

The eight-bit A-Bus selector (F9, D9, F8, D8, D5, and C5) selects the A input to the ALU during the execution of an inter-register micro-instruction. The selector is composed of a 48-line to 8-line multiplexer with tri-state outputs, 8-bit tri-state buffer for the WC register, and the tri-state outputs of the RAM. The A-Bus selector is controlled by the A-Source Decoder.
The following is a list of the inputs to the A-Bus Selector:

CPU A-Channel inputs, lower $\overline{SD1}$ - $\overline{SD8}$
CPU A-Channel inputs, upper $\overline{SD9}$ - $\overline{SD16}$
CPU Q-Channel inputs $\overline{ADR1}$ - $\overline{ADR4}$, $\overline{ADR6}$ and READ BUF signal
ROM outputs PR0 - PR7
Program Counter bits 0 - 7
B0Register outputs
WC Register outputs
RAM outputs.

A-Source Decoder

The A-Source Decoder consists of a selector at location A4 and a decoder/demultiplexer at location B8. When a jump micro-instruction is executed, PR15 will be low. This will select the A input of the selector at A4, causing IR (from A4-9) to go low and thus selecting PR0-PR7 as the outputs of the multiplexers at locations D5 and C5. Also the output of the AND gate (F2-6) will be driven low by the IR signal. This will enable the outputs of multiplexers D5 and C5 by placing a low signal on C5-15 and D5-15. Concurrently the IR signal will drive the inverter output at B2-12 high; thus disabling the outputs of the decoder (B8). The decoder outputs B8-5, B8-6 will go high and will disable the outputs of the WC register buffers (C7-1, C7-15 and C6-15 will be high) and will disable the tri-state outputs of the RAM (A6-8 and A7-8 will be high). With B2-12 high, the buffer outputs C6-9,5,3 and 7 will be disabled and will also be high. The function select pins of the ALU (GF7-6, 5,4, and 3) will be high. The ALU M input (GF7-8 and GF6-8) will be driven high by NAND gate output B3-8. With S0 - S3 and M inputs to the ALU high, the ALU will pass the PR0-PR7 data to ALU outputs GF7-9, 10, 11 and 13 and GF6-9, 10, 11 and 13.

For an inter-register micro-instruction, B2-12 is low. The B8 decoder is enabled and PR0, PR1 and PR2 provide the data for the decoder select inputs (B8-2,3 and 14). When the selected source is the RAM, B8-12 is low; A6-8 and A7-8 are low. When the "Write Character for PTP" Register is the selected source, B8-11 is low, C7-1, C7-15 and C6-15 are low.

Program Counter

Three synchronous 4-bit counters (D7, D6 and B5) provide a ten-bit address for the 1024 word PROM. This program counter receives its lower eight bits from the ALU/Out bus. The two most significant bits are loaded from a two-bit return address register which is used for returning from subroutines or from PRO8 and the output of the RAM Bank Select F/F (RMBNKS). The multiplexer at A4 selects the input to the two most significant bits of the PC. During a jump to Subroutine operation, the lower eight bits of the PC are saved in address 0 of the Register File (RAM) and the upper two bits of the PC are saved in the two-bit return address at A3. During subroutine returns, the upper two bits of the PC are loaded from the two flip-flops at A3 by the A4 selector. The lower eight bits are loaded from RAM0. Receipt of a low signal on the Load PC line (D7-9, D6-9 and B5-9) will cause the PC to be loaded on the trailing edge of $\overline{\emptyset 0}$. The PC outputs are connected to PROM address and to A-Bus Selector.

PROM (Programmable Read Only Memory)

The PROM is organized as an array of 512 words by 8 bits.

Four PROM's are used to construct a micro-memory of 1024 words by 16 bits.

The nine address bits of the PROM are provided by the nine lower Program Counter bits. The tenth bit of PC selects between the lower 512 word bank (CD1, CD3) and the upper 512 word bank (CD2, CD4). When B5-13 is low, the lower bank is selected (CD1-20, 21 and CD3-20, 21 are low); when B5-13 is high, the upper bank is selected (CD2-18, 19 and CD4-18, 19 are high).

The 16-bit tri-state outputs of the upper and lower PROM banks are wire-ORed together.

The PROM PRO-PR7 bits provide an A-source for the A-bus selector. PROM bits are also connected to various circuits to generate and control microprogram execution.

B-Register

The B-Register (locations E6 and E7) is a general purpose 8-bit register on the A-side of the controller. ALU-out bus data is multiplexed at the input to the B-REgister with receivers of input pins 29, 28, 37, 30, 33, 38, 31 and 34.
Flip-flop G1-6 (SELBREG) slects the input to the B-Register. The trailing edge of $\overline{\text{BREGD}}$ pulse (from K2-6) strobes the selected data into the register. The B-Register outputs are connected to the A-Bus Selector. The B REG 2^5 (BMDL) and B REG 2^7 bits (BMSB) are connected to jump conditions at E1-14 and F1-1 respectively.

"Write Character for PTP" Register

Two synchronous 4-bit Up-Down counters at B6 and B7 constitute the WC Register. This circuit is used as a Down Counter for Delay Time circuit, and as a register for PTP Punch Data. During a DELAY TIME operation teh counter counts down until WCEMPT (B6-13) goes low. The $\overline{\text{WCD}}$ pulse loads the WC Register. The WC Register outputs are connected as an A-side source through tri-state buffers at C7 and C6. Also, the WC-Register outputs are connected via drivers at A8A, C8B, C9B, C8A and C9A to pins 7, 18, 12, 14, 15, 19, 13, 17 and 11 respectively. This allows the WC to be used as a data to device register. The drivers are enabled and the Write Data is placed on the lines only when the ONBUSFF flip-flop (A1-9) is set.

RAM (Random Access Memory)

Two 16x4 clocked RAM's with tri-state latched outputs (at A6 and A7) constitute the File of the Controller.
The address of the file is selected by a 4-bit RAM Address Register. The data to be written into the file is received from the ALU-out Bus. The RAM tri-state outputs are connected as a source to the ALU-A-input.

An active low $\overline{\text{RAMD}}$ (from L2-9) pulse acts as a Write pulse at A6-2 and A7-2 during the time that A6-7 and A7-7 are held low. The timing diagram illustrates the operation mode of the file (Fig. 5-3).
The transition of CP from low to high causes the contents of the file location selected by the Address Inputs (A0-A3) to be strobed into the file Output Register. A tri-state Output Enable ($\overline{\text{EO}}$) controls the Output Buffers. When $\overline{\text{EO}}$ (A6-8, A7-8) is low, the outputs are determined by the data in the output register.

RAM Address Register

The quadruple D-type flip-flops at A5 are used as the RAM Address Register. This register is loaded from the ALU-out bus with the address of the file register. The loading is executed on the trailing edge of a $\overline{\text{RAMADD}}$ (L2-11) active low pulse.

Arithmetic Logic Unit

The heart of the Cyber 18 Device Controller comprises an 8-bit ALU (GF7 and GF6). The ALU is fed on the A-side by the A-Bus Selector which selects one of eight source A inputs. On the B side of the ALU, the B-Bus Selector selects one of four source B inputs. The ALU output bus is routed to one of 12 destination registers and to a parity generator/checker. The ALU performs sixteen binary arithmetic operations which are selected by four function select lines (S0, S1, S2 and S3). The function select lines are received from the PROM through buffers (C6). These buffers are enabled during the execution of an inter-register instruction. In this case, the Data Selector/Multiplexer (A4) generates an IR signal: PR15 (A4-1) is high; PR14 (A4-10) is high; IR (A4-9) is high. The IR signal is inverted by inverter B2-13/12 and provides an enable for C6-1. The Internal Carry (GF7-7) is provided by flip-flop CNALU (A1-12). PR3 is enabled by the IR signal (B3-9) and inverted (B3-8). The output of the inverter supplies the input for the ALU (GF7-8, GF6-8).
The inverted Carry Output of the first ALU (GF7-16) is provided as a Carry Input to the second ALU (GF6-7).

Parity Generator/Checker

The Controller includes a parity generator/checker at location R5. The Parity Generator/Checker is provided with the eight ALU-out bus bits. The ninth input (R5-4) is the flip-flop PARSUP (NT-12). The output of Parity Generator/Checker (R5-5) is latched at G5-13/8. G5-8 is connected to jump condition PARLTC (H7-14).

Carry Out, A=B, and Parity Latch

A 4-bit register at G5 is used as a latch for the ALU Carry Output (G5-2/4), for the ALU Comparator Output A=B (G5-1/6) and for the parity bit/error output (G5-13/8). During the execution of an inter-register micro-instruction, the IR signal will be high. This will cause the latch load input (G5-9) to be high. Data is strobed into the latch with the leading edge of clock phase $\overline{\emptyset 0}$. The latch data will remain valid until a new inter-register instruction is executed.

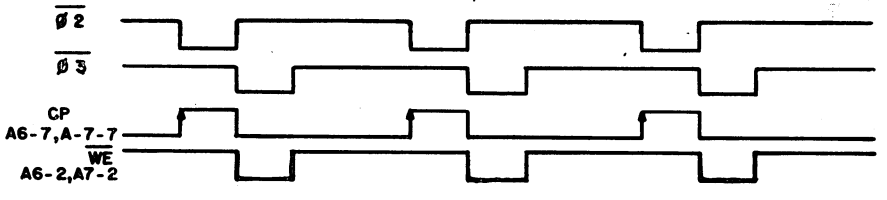


Figure 5-3. Timing for Operation Mode of File

NOTE

The A=B ALU open collector outputs (GF7-14 and GF6-14) are wired OR together to give comparison for eight bits. A pull-up resistor $S3_2$ is used for the wired OR connection.

B-Bus Selector

The Dual 4-line-to-1-line Data Selectors/ Multiplexers at J9, J8, J7 and J6 constitute the B-Bus Selector. The B sources are CWALS (CP Write Lower), CWAUS (CP Write Upper), BF2LS (Buffer 2 Lower), BF2US (Buffer 2 Upper). The PROM bits PR12 and PR13 select the B-side source during the execution of inter-register micro instructions.
The B-Bus Selector outputs are connected to the ALU B-inputs.

CWA (CP Write) Register

The synchronous 4-bit Up-Down counters K9, K8, K7 and K6 constitute the CWA Register. This register is divided in two sub-registers: CWA Low (K9, K8), CWA Up (K7, K6). The inputs of each sub-register are connected to the ALU-out bus. The CWA Low and CWA Up outputs provide the inputs for the B-side selector. The two-bit bank outputs (L6-3 and L6-2) are connected as Jump Conditions to M1-2 and M1-15 respectively. The CWA Reigster is used as a Card Punch Data register during card punching. This register provides the twelve bits of data through buffer gates to the connector pins. The tri-state buffer inverters L8 and L9 receive enable from J3-11 (jumper JM is inserted). L8-1, L8-15, L9-1 and L9-15 are low. The CP data bits are connected at pins 53 through 62, 253 and 254.

NOTE

In the PT/CP Controller, the Jumper Mode state is always low (the jumper is inserted).

All of the CP Data bits are active low signals.

The CWA Sub-registers are loaded from the ALU-out Bus. The CWA Low is loaded when an active low $\overline{\text{CWALD}}$ pulse from K2-13 is provided to K9-11 and K8-11. The CWA Up is loaded when an active low $\overline{\text{CWAUD}}$ pulse from K2-12 is provided to K7-11 and K6-11. Loading of the CWA register is done asynchronously with the counter clock.

Bank Register

The Bank is loaded when an active low $\overline{\text{BANKD}}$ pulse from L2-10 is provided to L6-11. Loading of the BANK register is done asynchronously with the counter clock.

Buffer 2 Register

The Buffer 2 register is composed of four 4-bit registers with multiplexed inputs at M7, N7, P7 and R7. The register is divided into two 8-bit sub-registers called Buffer 2 low (bits 7 - 0) and Buffer 2 up (bits 15 - 8). Bits 15 - 8 of the Buffer 1 register are multiplexed with the ALU-output bus at the input to Buffer 2 up. Bits 7 - 0 of the Buffer 1 register are multiplexed with the ALU-output bus at the input to Buffer 2 low. Flip-flop S5-12 selects the input to Buffer 2 low and Buffer 2 up. $\overline{\text{BF2LD}}$ (K2-10) and $\overline{\text{BF2UD}}$ (K2-9) active low pulses, constitute the loading pulses for Buffer 2. The outputs of the Buffer 2 Register are connected as sources (Buffer 2 Low - M7 and N7 and Buffer 2 Up - P7 and R7) to the B-side Selector. Also the Buffer 2 Register is connected through buffer gates to connector pins.

Bit Counter

The Bit Counter (L3) is provided with a clock input (L3-2) that is selected by the multiplexer at P3. Flip-flop ENDLCK (N1-11) is set; $\overline{\emptyset 0}$ is provided through P3-3/4 and F5-14/13 to L3-2. A high level at L3-15 indicates that the counter has counted 15 clocks. To extend the clock counting to 16 clock pulses, the carry output of the bit counter (L3-15) is connected to the Data input of the

D-flip-flop at N3-13. This carry out extension is controlled by the micro-program. Flip-flop ENDLOP (N1-9) enables Word Sync flip-flop activity (N3-13 will be high when flip-flop ENDLOP is set).

N3-9 is connected to B7-4. All 6.4 μsec (16 x 0.4 μsec), an active high pulse counts down the counter (WC register). The Jump Condition $\overline{\text{WCEMPT}}$ E1-1 indicates that the coutner is empty.

NOTE

For a Delay Time Operation, the WC Register is loaded with FF_{16}.

D-Type FF Circuit

This circuit is used to sense the leading/trainling edge of CP Busy and $\overline{\text{CPEOC}}$ signals. The CP Busy signal (pin 91) is inverted first by T9-13/12 and second by R4-9, 10/8 (JM is inserted). Initially flip-flop R3-2, 3,4/5 is set by Control Line CPINST (S2-9). The flip-flop is reset at the leading edge of CP Busy (R3-2 is low). R3-5 is connected to Jump Condition CPINFJC (R1-1).
The $\overline{\text{CPEOC}}$ signal (pin 92) is inverted first by T9-9/8 and second by R4-12, 13/11. Initially, flip-flop R3-12, 11, 10/9 is set by Control Line CPFEST (M2-9). The flip-flop is reset at the trailing edge of $\overline{\text{CPEOC}}$ (R3-12 is low). R3-9 is connected to Jump Condition CPFEDJC (R1-14).

Destination Decoder

The Decoder/Demultiplexers at L2 and K2 make up the Destination Decoder. The select inputs L2-1,2,3, and K2-1,2,3 are connected to PR8, PR9 and PR10. $\overline{\text{PR11}}$ enables L2-6 and PR11 enables K2-2 (thus choosing between the two decoders); $\overline{\text{Dest Decoder Enb}}$ from the AND gate (F2-8) enables L2-5 and K2-5. The active low pulse to clock the selected destination is generated when the clock phase $\overline{\emptyset 3}$ enables the L2-4 and K2-4 decoder input. The Controller uses 12 of 16 Destinations. The signal $\overline{\text{destination}}$ (active low pulse) enables the loading of the data into the designated register.

Control Lines

The Decoder/Demultiplexers at S2 and M2 comprise the Control Lines Decoder. The select inputs S2-1,2,3 and M2-1,2,3 are connected to PR8, PR9, and PR10. $\overline{\text{PR11}}$ enables S2-6 and PR11 enables M2-6 (thus choosing between the two decoders); $\overline{\text{MODE CL/FF}}$ from G2-11 Decoder/Demultiplexer enables S2-5 and M2-5. The active low pulse of the selected control line is generated when clock phase $\overline{\emptyset 3}$ enables the S2-4 and M2-4 decoder inputs.
The PT/CP Controller uses even of the sixteen control lines. Control Line 15 cannot be used due to the structure of the micro-program instruction.

Flip-Flop Network

The eight bit Addressable Latches (A2, S5, N1 F1, S1, A1, and B1) are multifunctional devices capable of storing single line data in eight addressable latches.
The addressable latch address inputs (pins 1, 2 and 3) are connected to PR0, PR1 and PR2 through the inverters G3-1/2, G3-3/4 and G3-5/6. PR12 determines the data to be stored: PR 12=1 sets the selected flip-flop; PR12=0 resets the selected flip-flop.
The Decoder/Demultiplexer at H1 enables the selected group of eight flip-flops. PR3, PR4 and PR5 select the group; $\overline{\text{PR0}}$, $\overline{\text{PR1}}$ and $\overline{\text{PR2}}$ select the flip-flop within the group. Group selection is enabled when the controller executes a CL/FF micro-instruction. An active low signal $\overline{\text{MODE CL/FF}}$ enables H1 (H1-5 goes low). The H1 outputs, which are connected to enable pins (pin 14) of each of the FF groups, generate an active low pulse on the selected output pin during the $\overline{\emptyset 3}$ clock phase at H1-4.

The groups 1,2,3,4 and 5 are connected to the $\overline{\text{CCMR2}}$ signal, and a $\overline{\text{General Reset}}$ ($\overline{\text{GR}}$) signal or a $\overline{\text{Clear Controller}}$ signal clears the flip-flops in these groups. The groups 6 and 7 are connected only to the $\overline{\text{GR}}$ signal, thus the Clear Controller command does not clear these two groups of flip-flops. The Controller Flip-Flop Network includes a total of fifty-six flip-flops.

Jump Condition Network

The eight-to-one data selector/multiplexers T1, R1, M1, H3, H7, F1, U7, E1, J1 and N2, the 2-input AND-OR invert gate at M5, the OR gate at K3-1,2/3, the two inverters at H2-5/6 and T3-11/10 and the flip-flop at H5 make up the Jump Condition Network.

There are nine groups of jump conditions. PR10, PR11 and PR12 select the Jump Condition within one of the nine jump condition groups. The bits PR10, PR11 and PR12 are inverted by H2-9/8, H2-11/10, H2-13/12 and connected to input pins 11, 10 and 9 of the T1, R1, M1, H3, H7, F1, U7 and E1 (jump condition groups 1 to 8) and J1 (group 9).

The jump condition groups 1 to 8 strobe inputs are constantly enabled via a connection to ground. The jump condition Group 9 is enabled by an active low signal at K3-3 (PR15 OR-ed with $\overline{\emptyset 3}$).

The PROM bits PR13, PR14 and PR9 select the Jump Condition group. The strobe to this selector (N2-7) comes from K3-3 when the controller executes a jump instruction (PR15 is low). The OR gate K3-1,2/3 provides this strobe signal with $\overline{\emptyset 3}$ pulse. The flip-flop JGRP9 (G1-11) controls the selecting of jump condition. When the flip-flop is reset, the controller selects the jump condition within the groups 1 to 8. When flip-flop JGRP9 is set, the micro-program selects the jump conditions in group 9 (J1). H2-5/6 inverter and M5-13,1,9,10/8 gate provide this selection. The state of S/R flip-flop at H5 depends on the state of the selected jump condition.

Also this S/R flip-flop at H5 is set by a $\overline{\text{PCD}}$ (L2-7) active low pulse, whenever the PC is the destination register for an inter-register instruction. The flip-flop output (H5-4) is inverted by T3-11/10 and provides the $\overline{\text{Load PC}}$ pulse for the Program COunter. The Program Counter will be loaded with the ALU-out data and the data selected by the multiplexer at A4, thus executing a micro-program jump. The $\overline{\text{Load PC}}$ signal is active during the time interval from the leading edge of clock phase $\overline{\emptyset 3}$ to the leading edge of the next $\overline{\emptyset 2}$ clock phase ($\overline{\emptyset 2}$ resets the S/R flip-flop at H5).

The Controller includes a total of seventy-two jump conditions.

TABLE 5-1. INPUTS FROM DEVICE

Signal Name	Pin Number	Termination Type	Receiver Location	Jump Condition Name and Location
PTR SC	25	220/330 ohms	E9-9/8	PTRSC (H7-1)
PTR SO	22	220/330	H9-5/6	PTRSO (H7-2)
PTR CA	20	220/330	E9-11/10, H8-4/13	PTRCA (H7-12)
PTR D1	29	220/330	E8-5/6	
PTR D2	28	220/330	E8-3/4	
PTR D3	37	220/330	E8-1/2	
PTR D4	30	220/330	E9-1/2	B REGISTER
PTR D5	33	220/330	E8-13/12	
PTR D6	38	220/330	E9-5/6	
PTR D7	31	220/330	E9-3/4	
PTR D8	34	220/330	E8-11/10	
PTR P	21	220/330	E9-13/12, H8-6/11	PTRPAR (H7-13)
PTP A0	24	220/330 ohms	H9-3/4	PTPAO (H7-3)
PTP AC	23	220/330	H9-1/2	PTPAC (H7-4)
PTP AM	16	220/330	H9-9/8	PTPAM (H7-15)
CP BUSY	91	470 ohms	T9-13/12	CPBSY (R1-12)
CP ERR	298	470	U9-13/12	CPECER (U7-14)
CP PINH	297	470	U9-9/8	CPPUIH (U7-1)
CP RDY	99	470	U8-13/12	CPRDY (R1-4)
CP STBY	95	470	U9-3/4	CPSTBY (U7-3)
CP HE	97	470	U9-11/10	CPHOEM (U7-15)

All input signals from devices are active-low.

TABLE 5-2. OUTPUTS FROM CONTROLLER TO DEVICES

(Numbers inside parentheses indicate notes)

Signal Name (1)	Origin	Driver Location	Pin Number
PTR AC	PTRAC	A9A-1,2/3	4
PTR AM	PTRAM	A9B-1,2/3	3
PTP SC	PTPSCFF	A9B-6,7/5	10
PTP CA	PTPCA	A8B-6,7/5	8
PTP P	PTPPAR	M9B-6,7/5	250
PTP D1	WC B7-3	C8A-1,2/3	11
PTP D2	WC B7-2	C9A-6,7/5	17
PTP D3	WC B7-6	C9A-1,2/3	13
PTP D4	WC B7-7	C8A-6,7/5	19
PTP D5	WC B6-3	C9B-6,7/5	15
PTP D6	WC B6-2	C9B-1,2/3	14
PTP D7	WC B6-6	C8B-1,2/3	12
PTP D8	WC B6-7	C8B-6,7/5	18
(2) CP PUNCH SEL	--	--	--
CP OFFSET	CPOFFS	S7A-1,2/3	82
CP FEED	Flip-Flop R3-9	S6A-1,2/3 (4)	81
CP INFO	Flip-Flop R3-5	S6A-6,7/5 (4)	85
(3) Punch Data Row 0	CWA K7-2	L8-14/13	62
Punch Data Row 1	CWA K7-3	L8-12/11	61
Punch Data Row 2	CWA K8-7	L8-6/7	60
Punch Data Row 3	CWA K8-6	L8-10/9	59
Punch Data Row 4	CWA K8-2	L9-14/13	58
Punch Data Row 5	CWA K8-3	L9-12/11	57
Punch Data Row 6	CWA K9-7	L9-10/9	56
Punch Data Row 7	CWA K9-6	L9-6/7	55
Punch Data Row 8	CWA K9-2	L9-2/3	54
Punch Data Row 9	CWA K9-3	L9-4/5	53
Punch Data Row 11	CWA K7-6	L8-4/5	253
Punch Data Row 12	CWA K7-7	L8-2/3	254

Notes:

1. All signals output from the controller to a device are active-low.
2. The Punch Select signal to the Card Punch device is held at the constant logical value of "0".
3. The insertion of jumper JM enables the outputs of the CP Punch Data Rows through J3-12, 13/11. The constant set of the On Bus Flip-Flop enables the other out put lines. See page 2-7.
4. Gate S6A-6, 7/5 (wired-OR to gate S6B-6, 7/5) and gate S6A-1, 2/3 (wired-OR to gate S6B1, 2/3) are enable by the insertion of jumper JM.

Unit Protect

The three devices are protected whenever the UPO jumper is inserted. The UPO jumper is located at P1 and is connected to the 4-input multiplexer at P2. The inverted output P2-14 is connected to jump condition UNTPRT (F1-14).

When jumper UPO is removed, all the three devices are non-protected.

Maintenance Switches

The LS switch is the ON-Off Line Switch and is connected to jump condition ONOFLN. In the "ON" position, the switch permits normal controller activity. In the "OFF" position the switch disconnects the controller from the A/Q bus of the computer and places the controller in the Maintenance mode. In this mode, the AND gate output U4-12 will be low. The sequencer input U6-4 will also be low thus disabling sequencer operation. Consequently, all A/Q commands received will generate an internal reject.

The type of operation performed is now a function of the positions of the maintenance switches (MS1-MS3).

MS1 is connected to jump condition MSW1 (J1-14).

MS2 is connected to jump condition MSW2 (J1-2).

TABLE 5-3. MAINTENANCE SWITCH POSITIONS

MS3	MS2	MS1	Off-Line Operation
Off	Off	Off	Not Used
Off	Off	On	Not Used
Off	On	Off	CP Triangular Data Pattern
Off	On	On	CP All Ones
On	Off	Off	PTP Triangular Data Pattern
On	Off	On	PTR Backward Motion
On	On	Off	PTR Forward Motion
On	On	On	Not Used

MICRO INSTRUCTION DESCRIPTION

Most of the control logic with the Controller is implemented by micro instructions contained with Programmable Read Only Memory (PROM). This design approach replaces the more conventional hard-wired random logic.

To understand the Controller's logic the reader must first understand how the micro-control section operates and then how to follow the logical program flow as shown in the flow charts.

The following description describes the micro-instruction and their implementation. The micro-program flow charts are shown in Appendix A.

The Microinstruction Repertoire

The microinstruction set is divided into 4 groups:

1. Inter-Register instructions.
2. Load Constant instructions.
3. Control Line and FF instructions.
4. Jump instructions.

The 16 bit microinstruction word is denoted R00 through R15, where R00 is the least significant bit. Figure 5-4 is a summary of the various microinstruction group formats.

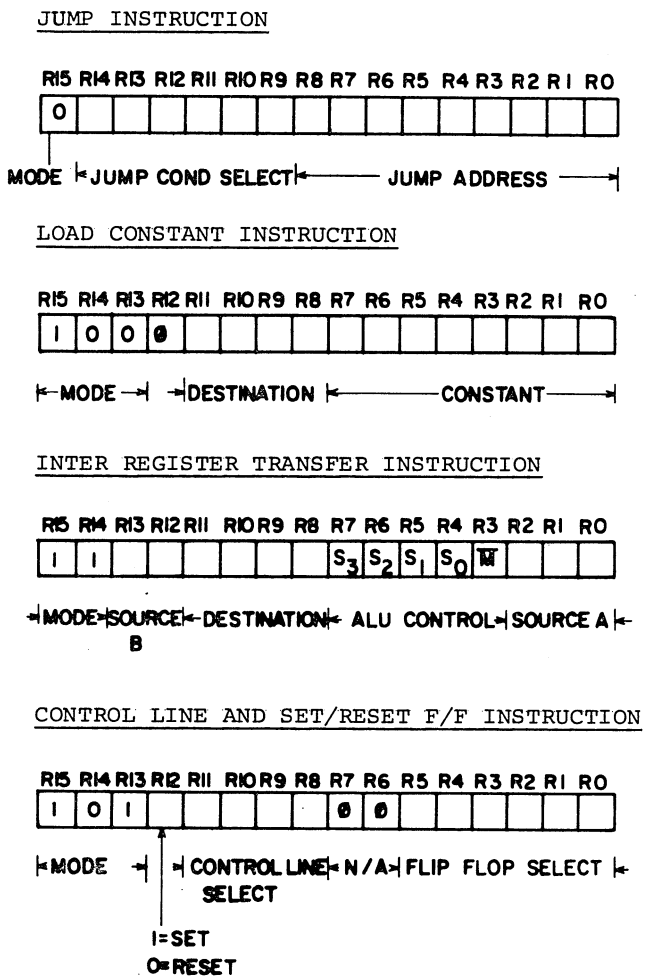


Figure 5-4. MICROINSTRUCTION GROUPS

Inter-Register Microinstruction

Inter-register microinstructions are identified by R14=1 and R15=1. These instructions cause data from a combination of two sources to be sent through the ALU to a destination register. Various logic and arithmetic operations, selected by the ALU control lines, are performed on the data as it passes through the ALU. Figure 5-5 illustrates the instruction format.

The source A field bits R00, R01 and R02, select one of seven available source A registers. Table 5-4 provides the Source A codes.

The Source B field, bits R13 and R12, select one of four available Source B registers. Table 5-5 provides the Source B codes.

The Destination field, bits R08 through R11, select one of 12 destination registers. Table 5-6 provides the Destination codes.

The ALU Control field bits R03 through R07 activate five of the six ALU control lines. The remaining ALU control line Cn is activated by a control flip-flop. Table 5-7 provides the ALU operation codes.

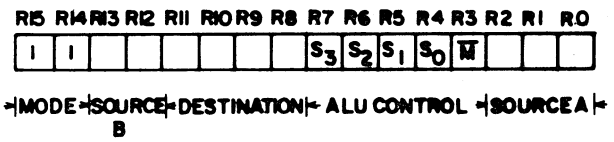


Figure 5-5. Inter-Register Microinstruction Format

Load Constant Micro-Instruction

The Load Constant microinstruction, identified by R13=0, R14=0 and R15=1, loads an 8-bit character (constant) originating from the PROM into one of 12 destination registers. Figure 5-6 shows the instruction format. Bits R08 through R11 select the destination register. Table 5-6 provides the destination register codes.

Jump Microinstruction

Jump type micro instructions are identified by R15=0. Figure 5-7 shows the Jump Micro instruction format.

The bits R08 through R00 specify the Jump Address. The 1K PROM is divided into 2 banks of 512 words each (locations 0-511 are called the lower bank, locations 512-1023 are called the upper bank). R08-R00 specify the address within a bank. The ROM Bank Select (RMBNKS) F/F, which is set or reset by the Flip-Flop/Control Line Instruction, selects the bank to which the jump will be made.

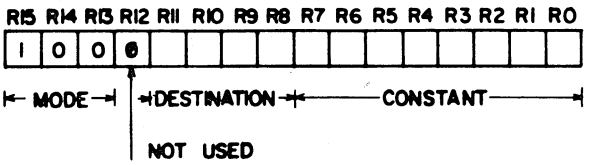


Figure 5-6. Load Constant Microinstruction Format

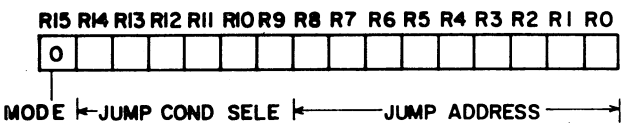


Figure 5-7. Jump Microinstruction Format

The Jump condition select field consists of bits R14 through R09. There are seventy two available jump conditions divided into two groups of sixty four and eight. The jump condition group (JGRP9) ENB FF, which is set or reset by the FlipFlop/Control Line Instruction, selects the group. Bits R14-R09 select the condition within the group. (For the Group of 8, only R11-R09 are valid.) Table 5-11 shows the Jump condition select codes and the corresponding jump conditions.

There are two types of Jump Instructions:

A) Unconditional Jump: This type is identified by R14-R09 equal zero. The program counter bits 8-0 will be loaded with R08-R00. Program counter bit 9 will be loaded with the contents of ROM Bank select (RMBNKS) F/F.

B) Conditional Jump: If the selected condition is true, the program counter will be loaded with R08-R00 and the Bank select (RMBNKS) F/F. If the selected condition is false, the program counter will be incremented by one.

Jumping to Subroutines

Jumping to subroutines is a two-step process. First the return address must be saved, and then a jump (conditional or unconditional) must be made to the starting address of the subroutine. (The Bank Select (RMBNKS) F/F must be set according to the bank in which the subroutine is located prior to the jump.) Figure 5-8 shows the instruction sequence necessary for jumping to and returning from subroutines. P incremented by one (P+1) is loaded into the register file at address 0 via an inter-register instruction. Address 0 is provided to the File Address Register (RAMADD) by the hardware. Execution of this instruction will also cause the upper two bits of the PC to be saved in flip-flops. Next, a jump is executed to the starting address of the subroutine. To return from the subroutine zero is loaded into the File Address Register (RAMADD) via a load constant instruction. The contents of RAM 0 is incremented by one and loaded into the PC. This causes a jump to the return address (P+2). The upper two bits which were saved in flip-flops are loaded into the upper bit positions by hardware.

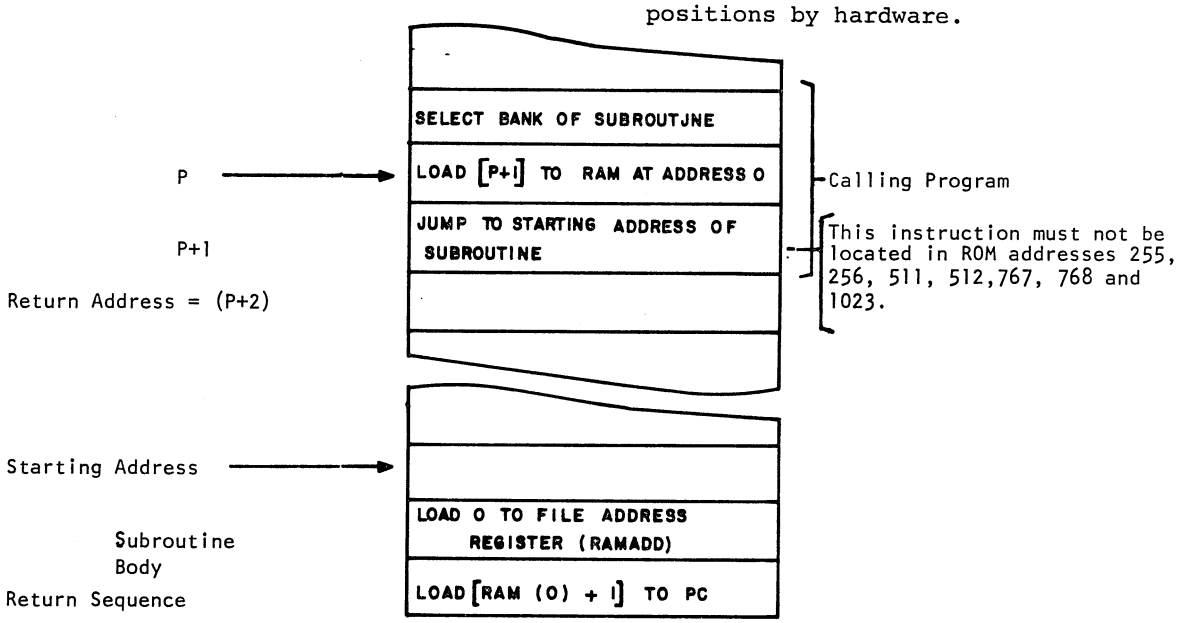


Figure 5-8. INSTRUCTION SEQUENCE FOR JUMPING TO AND RETURNING FROM SUBROUTINES

The Jump Instruction which causes the jump to the starting address of the subroutine cannot be located in PROM addresses 255, 256, 511, 512, 767, 767, or 1023 due to the structure of the PC.

Control Line and Set/Reset FF Instructions

These instructions identified by R13=1, R14=0 and R15=1, are used for setting or resetting one of the 56 available control flip-flops and for providing a pulse on one of 16 available control lines. Both of these operations can be performed in the same micro-instruction. Figure 5-9 illustrates the instruction format.

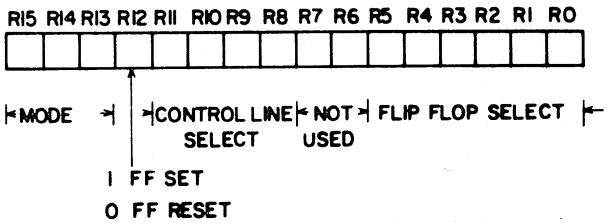


Figure 5-9. Control Line and Set/Reset FF Instruction Format

The Flip-Flop Select Field, R00 through R05 selects one of 56 available flip-flops. Table 5-9 provides the flip-flop codes. Bit R12=0 resets the selected flip=flop. Bit R12=1 sets the selected flip-flop.

The Control Line Select field selects one of 16 available control lines which will be strobed. Table 5-10 provides the control line codes.

TABLE 5-4. SOURCE A CODES

SOURCES = R15 R14

R02	R01	R00	SOURCE A
0	0	0	(FILE) RAMS
0	0	1	(WRITE CHARACTER) WCS
0	1	0	(A-LINES LOW) AINLS
0	1	1	(A-LINES UP) AINUS
1	0	0	(B-REGISTER) BREGS
1	0	1	(Q-LINES) QS
1	1	1	(PROGRAM COUNTER) PCS

Source A is the PROM in Load Constant Instruction (R15, $\overline{R14}$, $\overline{R13}$).

TABLE 5-5. SOURCE B CODES

R13	R12	SOURCE B
0	0	(CWA_L) CWALS
0	1	(CWA_U) CWAUS
1	0	(BUF 2_L) BF2LS
1	1	(BUF 2_U) BF2US

TABLE 5-6. DESTINATION REGISTER CODES

DESTINATION NUMBER	MICRO-INSTRUCTION FIELD				DESTINATION
	R11	R10	R9	R8	
0	0	0	0	0	NOT USED
1	0	0	0	1	NOT USED
2	0	0	1	0	NOT USED
3	0	0	1	1	NOT USED
4	0	1	0	0	FILE ADDRESS REGISTER (RAMADD)
5	0	1	0	1	CWAuu (CPU MEMORY BANK)(BANKD)
6	0	1	1	0	FILE (RAMD)
7	0	1	1	1	PROGRAM COUNTER (PCD)
8	1	0	0	0	WRITE CHARACTER (WCD)
9	1	0	0	1	A REG UPPER (AOUTUD)
10	1	0	1	0	CWA LOW (CWALD)
11	1	0	1	1	CWA UP (CWAUD)
12	1	1	0	0	A REG LOWER (AOUTLD)
13	1	1	0	1	BUF 2 LOW (BF2LD)
14	1	1	1	0	BUF 2 UP (BF2UD)
15	1	1	1	1	B REGISTER (BREGD)

TABLE 5-7. ALU CONTROL CODE INTER-REGISTER MICRO-INSTRUCTION

ALU CONTROL				LOGIC	ARITHMETIC	
S3	S2	S1	S0	M = 1	M=0, C_{in}=1	M=0, C_{in}=0
0	0	0	0	$\overline{A}$	A	A plus 1
0	0	0	1	$\overline{A+B}$	A+B	(A+B) plus 1
0	0	1	0	$\overline{A}\cdot B$	A+$\overline{B}$	(A+$\overline{B}$) plus 1
0	0	1	1	Logic 0	minus 1 (2s comp)	zero
0	1	0	0	$\overline{A\cdot B}$	A plus A$\cdot\overline{B}$	A plus A$\cdot\overline{B}$ plus 1
0	1	0	1	$\overline{B}$	A$\cdot\overline{B}$ plus (A+B)	A$\cdot\overline{B}$ plus (A+B) plus 1
0	1	1	0	A+B	A minus B minus 1	A minus B
0	1	1	1	A$\cdot\overline{B}$	A$\cdot\overline{B}$ minus 1	A$\cdot\overline{B}$
1	0	0	0	$\overline{A}$+B	A plus A$\cdot$B	A plus A$\cdot$B plus 1
1	0	0	1	$\overline{A+B}$	A plus B	A plus B plus 1
1	0	1	0	B	A$\cdot$B plus (A+$\overline{B}$)	A$\cdot$B plus (A+$\overline{B}$) plus 1
1	0	1	1	A$\cdot$B	A$\cdot$B minus 1	A$\cdot$B
1	1	0	0	Logic 1	A plus A=2xA	A plus A=2xA plus 1
1	1	0	1	A+$\overline{B}$	A plus (A+B)	A plus (A+B) plus 1
1	1	1	0	A+B	A plus (A+$\overline{B}$)	A plus (A+$\overline{B}$) plus 1
1	1	1	1	A	A minus 1	A

TABLE 5-8. FILE REGISTER USAGE

	RAM ADD REG				
(0)	0	0	0	0	Return Address
(1)	0	0	0	1	PTR INTRPT RSPNS
(2)	0	0	1	0	PTP INTRPT RSPNS
(3)	0	0	1	1	CP INTRPT RSPNS
(4)	0	1	0	0	PTR DATA & NRDY INTRPT REQ
(5)	0	1	0	1	PTP DATA & NRDY INTRPT REQ
(6)	0	1	1	0	CP DATA & NRDY INTRPT REQ
(7)	0	1	1	1	PTR STOP/START
(8)	1	0	0	0	PTR ASSY TRANSFER STAT
(9)	1	0	1	0	PTR SECOND CHARACTER REG
(10)	1	0	1	0	PTP INDEX CA
(11)	1	0	1	1	PTP FIRST CHARACTER REG
(12)	1	1	0	0	PTP SECOND CHARACTER REG
(13)	1	1	0	1	N/A
(14)	1	1	1	0	N/A
(15)	1	1	1	1	N/A

TABLE 5-9. FLIP FLOP CODES

FDD		R5	R4	R3	R2	R1	R0	PT/LP	I/O PIN
F/F GRP 1	0	1	1	0	1	1	1	———	5
	1	1	1	0	1	1	0	———	50
	2	1	1	0	1	0	1	PTPCA	8
	3	1	1	0	1	0	0	PTPCUFF	—
	4	1	1	0	0	1	1	RMBNKS	—
	5	1	1	0	0	1	0	PTPDSFF	—
	6	1	1	0	0	0	1	ECHO	7
	7	1	1	0	0	0	0	CPDATFF	—
F/F GRP 2	0	0	1	0	1	1	1		—
	1	0	1	0	1	1	0	———	81
	2	0	1	0	1	0	1	———	294
	3	0	1	0	1	0	0	CPOFFS	82
	4	0	1	0	0	1	1	———	85
	5	0	1	0	0	1	0	———	86
	6	0	1	0	0	0	1	———	87
	7	0	1	0	0	0	0	———	—
F/F GRP 3	0	0	1	1	1	1	1	———	—
	1	0	1	1	1	1	0	———	—
	2	0	1	1	1	0	1	———	—
	3	0	1	1	1	0	0	PTPPAR	250
	4	0	1	1	0	1	1	ENDLOP	——
	5	0	1	1	0	1	0	———	—
	6	0	1	1	0	0	1	ENDLCK	—
	7	0	1	1	0	0	0	PARSUP	—
F/F GRP 4	0	1	0	1	1	1	1	PTRDTFF	—
	1	1	0	1	1	1	0	BUSY	—
	2	1	0	1	1	0	1	SELBREG	—
	3	1	0	1	1	0	0	———	232
	4	1	0	1	0	1	1	———	—
	5	1	0	1	0	1	0	———	242
	6	1	0	1	0	0	1	JGRP9	—
	7	1	0	1	0	0	0	INTRSP	249
F/F GRP 5	0	0	0	1	1	1	1	———	—
	1	0	0	1	1	1	0	———	49
	2	0	0	1	1	0	1	———	88
	3	0	0	1	1	0	0	PTRAYFF	293
	4	0	0	1	0	1	1	———	—
	5	0	0	1	0	1	0	PTPSTFF	—
	6	0	0	1	0	0	1	PTRPEFF	—
	7	0	0	1	0	0	0	PTPIRFF	—

TABLE 5-9. FLIP FLOP CODES (Continued)

FDD			R5	R4	R3	R2	R1	R0	PT/CP	I/O PIN
F/F GRP	6	0	1	0	0	1	1	1	——	—
		1	1	0	0	1	1	0	——	9
		2	1	0	0	1	0	1	PTRAM	3
		3	1	0	0	1	0	0	PTPSCFF	10
		4	1	0	0	0	1	1	ONBUSFF	—
		5	1	0	0	0	1	0	——	84
		6	1	0	0	0	0	1	PTRAC	4
		7	1	0	0	0	0	0	CNALU	—
F/F GRP	7	0	0	0	0	1	1	1	——	227
		1	0	0	0	1	1	0	PTRBFFF	—
		2	0	0	0	1	0	1	PTPDYFF	—
		3	0	0	0	1	0	0	——	—
		4	0	0	0	0	1	1	EOP	—
		5	0	0	0	0	1	0	PTPDTFF	—
		6	0	0	0	0	0	1	PTRACFF	—
		7	0	0	0	0	0	0	CNTPRT	—

TABLE 5-10. CONTROL LINE CODES

C.L.	R11	R10	R9	R8	PT/CP
0	0	0	0	0	NOT USED
1	0	0	0	1	(SET REJECT) REJ
2	0	0	1	0	——
3	0	0	1	1	(SET REPLY) RPLY
4	0	1	0	0	(RST CP FD&INF) CPFIRT
5	0	1	0	1	——
6	0	1	1	0	(SET INFO) CPINST
7	0	1	1	1	PTRRT
8	1	0	0	0	——
9	1	0	0	1	——
10	1	0	1	0	——
11	1	0	1	1	——
12	1	1	0	0	(RT PTP DISASSY) PTPDYRT
13	1	1	0	1	——
14	1	1	1	0	(SET FEED) CPFEST
15	1	1	1	1	NOT USED

FLIP-FLOP CODES (Table 5-9)

FF 12: PTPCA - PTP Control Available.
Used when special control status information is transmitted using signals D1 through D8.

FF 13: PTPCUFF - PTP Cut Program.
Used as an index FF.

FF 14: RMBNKS - ROM Bank Select.
Used to jump between any of the S12 lower (upper) rom locations and any of the S12 upper (lower) ROM locations.

FF 15: PTPDSFF - PTP Disassembly Transfer Status.
Used to monitor data transfer status when disassembly data mode is selected.

FF 16: ECHO - Echo.
Used in Self Test 3 A/Q Command to allow echoed data transfer via the PT Relay Station.

FF 17: CPDATFF - CP Data Status.
Used as a flag for data transfer to the CP device.

FF 23: CPOFFS - CP Offset.
Used to offset the card moving from the punch station to the stacker in the CP device.

FF 33: PTPPAR - PTP Parity Bit.
Used to allow odd parity data transmission to the PTP device.

FF 34: ENDLOP - Enable Delay Operation.
Used to allow a delay of about 1 second when entering the Off-Line condition.

FF 36: ENDLCK - Enable Delay Clock.
Used together with FF 34.

FF 37: PARSUP - Parity Supplement.
Used for odd parity calculations.

FF 40: PTRDTFF - PTR Data Status.
Used as a flag for data transfer from the PTR device.

FF 41: BUSY - Controller Busy.
Used to inform the CPU that the controller is busy executing a CC, Self Test 1, Self Test 2 or Self Test 3 A/Q Command.

FF 42: SELBREG - Select B Register.
If this FF is set, B-Register is loaded from data coming from the PTR device; if this FF is reset, B-Register is loaded with data from the ALU.

FF 46: JGRP9 - Jump Conditions on Group 9.
Used to enable jump conditions on group 9.

FF 47: INTRSP - Interrupt Response.
This is the interrupt response line to the CPU.

FF 53: PTRAYFF - PTR Assembly Mode.
Used to select data transfer mode (Character/Assembly) from the PTR device.

FF 55: PTPSTFF - PTP Start Mode.
Used to allow data transfer to the PTP device.

FF 56: PTRPEFF - PTR Parity Error.
Used to inform the CPU (PTR Alarm Status A/Q Command) of any possible parity error on data transfer from the PTR device.

FF 57: PTPIRFF - PTP Info Ready.
Used as a flag to indicate that a PTP Data A/Q command is issued.

FF 62: PTRAM - PTR Acceptor Message.
Used to select direction of reading in the PTR device.

FF 63: PTPSCFF - PTP Source Control.
Used to start punching data on the PTP device.

FF 64: ONBUSFF - Enable bus to devices.
Used to enable output drivers.

FF 66: PTRAC - PTR Acceptor Control.
Used to request information on the data lines from the PTR device.

FF 67: CNALU - CN ALU.
Used to select logical or arithmetical ALU-operations.

FF 71: PTRBFFF - PTR B-Register Full.
Used to denote that one data character has been received from the PTR device.

FF 72: PTPDYFF - PTP Disassembly Mode.
Used to select data transfer mode (character/disassembly) to the PTP device.

FF 74: EOP - End of Operation.
Used to indicate the END point of Self Test 1, Self Test 2 and Self Test 3 A/Q commands.

FF 75: PTPDTFF - PTP Data/Function Status.
Used as a flag for data transfer to the PTP device.

FF 76: PTRACFF - PTR AC Index.
Used together with FF 62.

FF 77: CNTPRT - Controller Protect.
This FF is sampled only after every CC or MC.

TABLE 5-11. JUMP CONDITION CODES

	R15	R14	R13	R12	R11	R10	R9	PT/CP	I/O PIN
JC 10	0	0	0	1	1	1	0	PTRAYJC	(293)
11	0	0	0	1	1	0	0	PTRPEJC	——
12	0	0	0	1	0	1	0	PTPIRJC	——
13	0	0	0	1	0	0	0	PTPSTJC	——
14	0	0	0	0	1	1	0	——	291
15	0	0	0	0	1	0	0	RMEXEC	——
16	0	0	0	0	0	1	0	——	92
17	0	0	0	0	0	0	0	H (UCND JUMP)	——
JC 20	0	1	0	1	1	1	1	CPRDY	99
21	0	1	0	1	1	0	1	——	——
22	0	1	0	1	0	1	1		93
23	0	1	0	1	0	0	1	CPINFJC	(85)
24	0	1	0	0	1	1	1	——	42
25	0	1	0	0	1	0	1	CPFEDJC	(81)
26	0	1	0	0	0	1	1	ONOFLN	——
27	0	1	0	0	0	0	1	CPBSY	91
JC 30	0	0	1	1	1	1	1	——	——
31	0	0	1	1	1	0	1	——	——
32	0	0	1	1	0	1	1	——	35
33	0	0	1	1	0	0	1	——	——
34	0	0	1	0	1	1	1	——	36
35	0	0	1	0	1	0	1	——	——
36	0	0	1	0	0	1	1	——	——
37	0	0	1	0	0	0	1	——	296
JC 40	0	0	0	1	1	1	1	EQUAL	——
41	0	0	0	1	1	0	1	$\overline{\text{COUT}}$	——
42	0	0	0	1	0	1	1	——	237
43	0	0	0	1	0	0	1	——	44
44	0	0	0	0	1	1	1	——	——
45	0	0	0	0	1	0	1	——	252
46	0	0	0	0	0	1	1	——	263
47	0	0	0	0	0	0	1	——	48
JC 50	0	1	1	1	1	1	0	PTPAC	23
51	0	1	1	1	1	0	0	PTPAO (PTP RDY)	24
52	0	1	1	1	0	1	0	PTRSO (PTR RDY)	22
53	0	1	1	1	0	0	0	PTRSC	25
54	0	1	1	0	1	1	0	PTPAM	16
55	0	1	1	0	1	0	0	PARLTC	——
56	0	1	1	0	0	1	0	PTRPAR	21
57	0	1	1	0	0	0	0	PTRCA	20

TABLE 5-11. JUMP CONDITION CODES (Continued)

	R15	R14	R13	R12	R11	R10	R9	PT/CP	I/O PIN
JC 60	0	1	0	1	1	1	0	——	80
61	0	1	0	1	1	0	0	——	——
62	0	1	0	1	0	1	0	PTRDTJC	——
63	0	1	0	1	0	0	0	BMSB	——
64	0	1	0	0	1	1	0	PTRBFJC	——
65	0	1	0	0	1	0	0	UNTPRT	——
66	0	1	0	0	0	1	0	PTRACJC	——
67	0	1	0	0	0	0	0	PTPDTJC	——
70	0	1	1	1	1	1	1	——	94
71	0	1	1	1	1	0	1	CPSTBY	95
72	0	1	1	1	0	1	1	——	——
73	0	1	1	1	0	0	1	CPPUIH	297
74	0	1	1	0	1	1	1	CPHOEM	97
75	0	1	1	0	1	0	1	CPECER	298
76	0	1	1	0	0	1	1	——	98
77	0	1	1	0	0	0	1	——	299
JC 80	0	0	1	1	1	1	0	$\overline{\text{ONBUSJC}}$	——
81	0	0	1	1	1	0	0	PTPDSJC	——
82	0	0	1	1	0	1	0	PTPSCJC	10
83	0	0	1	1	0	0	0	$\overline{\text{WCEMPT}}$	——
84	0	0	1	0	1	1	0	PTPDYJC	——
85	0	0	1	0	1	0	0	BMDL	——
86	0	0	1	0	0	1	0	PTPCUJC	——
87	0	0	1	0	0	0	0	CPDATAJC	——
JC 90*	0	0	0	1	1	1	0	——	295
91	0	0	0	1	1	0	0	——	27
92	0	0	0	1	0	1	0	MSW2	——
93	0	0	0	1	0	0	0	MSW3	——
94	0	0	0	0	1	1	0	——	——
95	0	0	0	0	1	0	0	MSW1	——
96	0	0	0	0	0	1	0	——	——
97	0	0	0	0	0	0	0	——	——

* NOTE: JC Group 9- ENB F/F must be set.

JUMP CONDITION CODES (Table 5-11)

JC 10: PTRAYJC - PTR Assembly Mode.
Used together with FF 53.

JC 11: PTRPEJC - PTR Parity Error.
Used together with FF 56.

JC 12: PTPIRJC - PTP Info Ready.
Used together with FF 57.

JC 13: PTPSTJC - PTP Start Mode.
Used together with FF 55.

JC 15: RMEXEC - ROM EXEC.
Used to detect the beginning of an A/Q command.

JC 17: H - High.
Used for unconditional jumps.

JC 20: CPRDY - CP Ready.
Used to detect the ready condition from the CP device.

JC 23: CPINFJC - CP Info Ready.
Used to detect the starting point of the punching cycle in the CP device.

JC 25: CPFEDJC - CP Feed.
Used to detect the end of a Feed command.

JC 26: ONOFLN - ON/OFF LIne Switch.
Used to detect the position of the ON/OFF Line Switch.

JC 27: CPBSY - CP Busy Signal.
Used to detect punching time in the CP device.

JC 40: EQUAL - ALU A=B.
Used to detect if the contents of one register on the 'A' side equals the contents of a second register on the 'B' side.

JC 41: $\overline{\text{COUT}}$ - Carry Out.
Used to detect the ALU C-OUT signal value.

JC 50: PTPAC - PTP Acceptor Control.
Used to detect request of information from the PTP device.

JC 51: PTPAO - PTP Acceptor Operable.
Used to detect Ready condition from the PTP device.

JC 52: PTRSO - PTR Source Operable.
Used to detect Ready condition from the PTR device.

JC 53: PTRSC - PTR Source Control.
Used to detect the time when data coming from the PTR device is ready to be taken.

JC 54: PTPAM - PTP Acceptor Message.
Used to detect a message from the PTP device.

JC 55: PARLTC - Parity Latched.
Used for odd parity computations.

JC 56: PTRPAR - PTR Parity Bit.
Used to check odd parity condition on data from the PTR device.

JC 57: PTRCA - PTR Control Available.
Used only for Self Tests Operations.

JC 62: PTRDTJC - PTR Data Status.
Used together with FF 40.

JC 63: BMSB - B-Register Bit 2^7.
Used to check value of most significant bit of B-register.

JC 64: PTRBFJC - PTR B-Register Full.
Used together with FF 71.

JC 65: UNTPRT - Units Protected.
Used to detect protect condition on the three devices (PTR, PTP, & CP).

JC 66: PTRACJC - PTR AC Index.
Used together with FF 76.

JC 67: PTPDTJC - PTP Data Status.
Used together with FF 75.

JC 71: CPSTBY - CP Stand-By.
Used to detect the Stand-By condition in the CP device.

JC 73: CPPUIH - CP Punch Inhibit.
Used to detect the Punch-Inhibit condition in the CP device.

JC 74: CPHOEM - CP Hopper Empty.
Used to detect the Hopper Empty condition in the CP device.

JC 75: CPECER - CP Echo Error.
Used to detect the Echo-Error condition in the CP device.

JC 80: $\overline{\text{ONBUSJC}}$ - Enable Bus to Devices.
Used together with FF 64.

JC 81: PTPDSJC - PTP Data Status.
Used together with FF 15.

JC 82: PTPSCJC - PTP SC Index.
Used together with FF 63.

JC 83: $\overline{\text{WCEMPT}}$ - Word Counter Empty.
Used to detect the time when the contents of the WC register can be changed.

JC 84: PTPDYJC - PTP Disassembly Mode.
Used together with FF 72.

JC 85: BMDL - B-Register bit 2^5.
Used to check the value of B-Register bit 2^5.

JC 86: PTPCUJC - PTP Cut Program.
Used together with FF 13.

JC 87: CPDATAJC - CP Data Status.
Used together with FF 17.

JC 92: MSW 2 -Maintenance Switch 2.
Used to detect Off-Line Maintenance Operations code.

JC 93: MSW 3 - Maintenance Switch 3.
Used to detect Off-Line Maintenance Operations code.

JC 95: MSW1 - Maintenance Switch 1.
Used to detect Off-Line Maintenance Operations code.

PAPER TAPE RELAY STATION

LOGIC CIRCUIT DESCRIPTION

The PT Relay Station Printed Circuit contains the logic networks which interface the Cyber 18 PT/CP Controller with the Facit Paper Tape Reader and Punch devices.

Paper Tape Reader Connection Circuits

The data (PTR D1-PTR D8) from the Facit-4020 Paper Tape Reader is received at eight pins of connector J2: T, 17, U, S, 15, 16, R and P and conform to the requirements of the device output signals interconnection (SP1 interface). The data from Reader is received by a network of diodes, resistors and capacitors. In this mode, the input signals are high and are limited at +5V DC.

The data is transferred through Schmitt-Trigger inverters (IC 1, IC 2) and inverters (IC 12, IC 13) to Quad 2-input Multiplexers (IC 8 and IC 30). Whenever the Select inputs (IC 8-1 and IC 30-1) are Low, the PTR Data is transferred to the Multiplexers outputs.

This data is inverted and transmitted to the Controller by the Drivers at locations 9A, 9B, 20A and 20B. The output network consists of two resistors: 220 Ω and 330 Ω and all output signals to the Controller are active low. When the Relay Station is in the Copy mode the "Output to Controller" Drivers are disabled (Low at the input).

The IC 8 and IC 30 Multiplexer outputs are connected to IC 5 and IC 16 Quad 2-input Multiplexers. Whenever the Relay Station is in the Copy mode (IC5-1 and IC16-1 are Low), the data received from the Reader is transferred to IC 5 and IC 16 outputs. This data is transmitted through the 3-State Buffers IC 4, IC 26 and resistor networks (2.2K to Vcc, 47 Ω serial) to output pins B, J, 7, 4, 6, 5, E and D of J2 connector as Paper Tape Punch Data.

NOTE

The output resistor networks conform to the PTP input signals connection requirements.

The PTR control signals PTR P and PTR CA are received from Reader at pins 13 and 14 (J2). These signals are transmitted to the Controller or to the Paper Tape Punch (pins 8 and C at J2) in the same manner as the data. The signals are connected to Multiplexer IC17. The Multiplexer outputs are connected to drivers at location 6B. Whenever the Relay Station executes a Copy, the PTR P and PTR CA are transmitted through Multiplexer IC 27 and 3-State Buffers IC 26, to the Paper Tape Punch. PTR SO and PTR SC (pins M and N at J2) are received at the special networks which are required by the device output signal connection. These networks (resistors, capacitor, transistor, inverters, feedback resistor) constitute Schmitt-Trigger circuits.

The PTR SO and PTR SC signals are transmitted to Controller through Multiplexer IC 17 and drivers at location 6A. Whenever the Relay Station executes a Copy, the signals are transmitted through Multiplexer IC 27, 3-State Buffers IC 26 and resistor networks to Paper Tape Punch (pins F and H of J2).

The control signals to the Reader (PTR AO, PTR AM and PTR AC) are transmitted at pins K, L and 9 of connector J2. The output

networks (two resistors) conform to device input signals connection requirements. The output drivers IC3-4/5 and IC3-10/9 are constantly enabled (IC3-1 is grounded). IC3-12/11 is disabled for an Echo operation. In this case, the input at pin "u" of J1 connector is "low"; through IC 25-9/8 and IC 24-9,10/8 (the Copy switch is OFF) IC3-15 is "high" and disables IC3-12/11.

Whenever the Relay Station executes a Copy, the PTP AO, PTP AM and PTP AC signals are transmitted from pins J2-10, 12, 11 through Schmitt-Trigger networks, Multiplexer IC15 and Multiplexer IC14 to the Reader as PTR AO, AM and AC.

Whenever the Relay Station interfaces between the Controller and Reader, the PTR AM and AC signals are received at J1-h and d. Through IC18-3/4 and IC18-11/10 these signals are connected to the B input of the Multiplexer IC14. PTR A0 is the output signal of AND gate IC24-9,10/8 inverted by IC13-3/4 and connected at IC14-3. Only when the Relay Station executes an Echo operation (IC24-10 is high, IC24-9 is high) the PTR AO to device is low and the Reader is disconnected from Controller.

Paper Tape Punch Connection Circuits

The control signals from the Punch, PTP AM, PTP AM and PTP AC are received and connected as described above, for a Copy operation.

Whenever the Relay Station interfaces between the Punch and the Controller, IC15 Multiplexer output signals are transmitted through 21A, 21B Drivers and 220/330 Ω resistor networks to pins J1-N, M and P.

The data for punching (PTP D1 - PTP D8) is received from the Controller at pins J1-k,m a, z, 1, b, c and j. The punch data is connected at the B-inputs of IC5 and IC16 Multiplexers through 220/330 Ω resistor networks and Schmitt-Trigger inverters IC7 and IC18. Whenever the Relay Station is not in a Copy operation, the data from the Controller is selected by IC5 and IC16. The outputs of these Multiplexers are connected to output Buffers (IC4, IC26) and to Multiplexers IC8 and IC30. Whenever the Relay Station is in an Echo mode, the output Buffers to Punch (IC4, IC26) are disabled. IC8 and IC30 output signals are transmitted to the Controller through Drivers at 9A, 9B, 20A, 20B and resistor networks. The control signals to the Paper Tape Punch PTP P (J1-f), PTP CA (J1-e) and PTP SC (J1-s) are received, through resistor networks (220/330 Ω) and Schmitt-Trigger inverters IC18-5/6, IC18-9/8 and IC25-11/10, at the B-input of Multiplexer IC27. The signal at IC24-8 (COPY·ECHO) is inverted by IC13-3/4 and connected to IC27-10 as PTP SO. The Multiplexer IC27 outputs are connected through IC26 Buffer and resistor networks (2.2K connected to Vcc and 47 Ω in series) to pins 8 (PTP P), C (PTP CA), F (PTP SO) and H (PTP SC) of connector J2.

In an Echo mode, the outputs to the Punch are disabled, IC27 outputs are connected through Multiplexer IC17, Drivers at 6A and 6B and resistor networks (220/330 Ω) to the Controller (pins t, n, r and p of J1).

The control signals from the Paper Tape Punch PTP AO, PTP AM and PTP AC are transmitted to the Controller through Schmitt-Trigger networks, Multiplexer IC15, Drivers at 21A and 21B and resistor networks (220/330 Ω). The outputs are at pins N, M and P of connector J1.

Connections to Controller

The Controller requests active low signals from the devices. The signals transmitted by the Controller are active low. The devices request and transmit active high pulses.

The Relay Station matches the activity of the signals between the devices and the Controller.

The signals to and from Controller are connected at connector J1. The signals from the Controller are received by resistor networks and Schmitt-Trigger inverters. The signals to the Controller are transmitted by Drivers with resistor networks at the outputs. All these resistor networks are formed from 220 Ω and 330 Ω. The signal $\overline{\text{COPY}}$ disables the outputs to the Controller. In COPY mode the Controller is disconnected from the Relay Station.

For signal $\overline{\text{ECHO}}$ at J1-u, the Relay Station transfers the PTP Data and Control signals from the Controller as PTR Data and Control signals back to the Controller. In $\overline{\text{ECHO}}$ mode the Controller is disconnected from the devices.

Front Panel Switch and Display

On the Front Panel, a LED indicator illuminates whenever the Logic circuit receives +5V DC.

The Copy switch, whenever it is in the ON state, determines a Copy mode of operation.

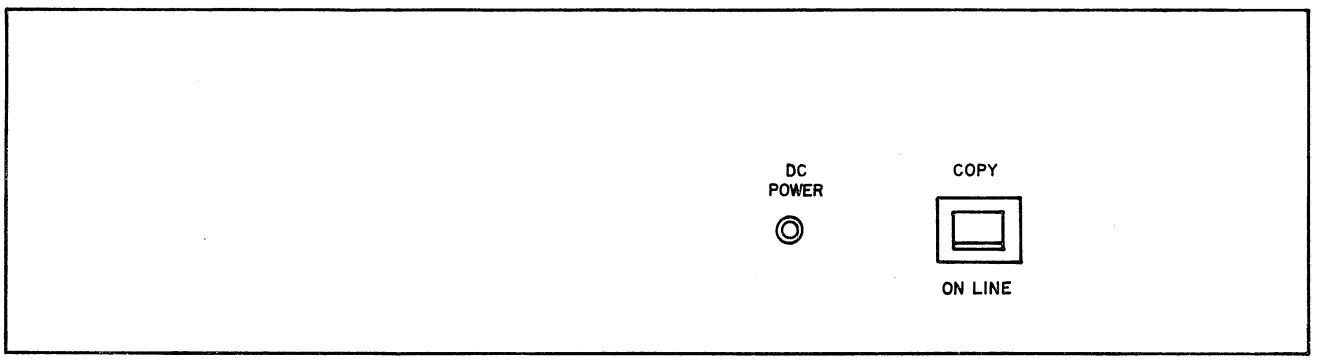


Figure 5-10. Paper Tape Relay Station Front Panel

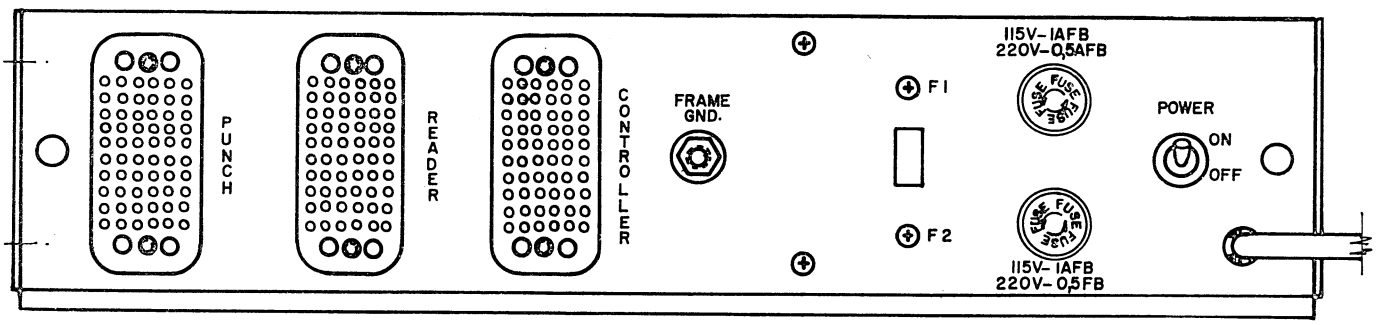


Figure 5-11. Paper Tape Relay Station Rear Panel

PT RELAY STATION POWER SUPPLY

The power supply consists of a transformer, a capacitor (CEXT), and a PWA circuit. The power supply provides the =5vdc for the Paper Tape Relay Station logic circuit.

The transformer lowers the 230 v/115v AC voltage to 22.0. A 230v/115v slide switch selects between the AC power input modes 230 or 115 VAC.

The secondary of the transformer is connected to an AC to DC rectifier. This circuit consists of two diodes CR17 and CR20 and two electrolytic capacitors C25 and CEXT.

The PWA includes a switching power supply. Transistor Q9 is switched by an active high pulse at the base. When Q9 conducts the choke T1 transfers current to the output. The voltage drop across the choke is 25v (+30v at end 1, +5v at end 2); T1 collects 5/6th of the total energy. WHenever Q9 ceases to conduct, the voltage at end 1 of T1 tends to "-∞".

$$V = L \frac{dI}{dt} \quad ; \quad I \rightarrow 0$$

$$\frac{dI}{dt} \rightarrow -\infty$$

$$V \rightarrow -\infty$$

Diode CR29 is a clamping diode and CR21 limits the voltage drop to "-0,7v".

The electrolytic capacitors C22, C23 and C24 form the output filter

Comparator U34-8,9/14, capacitor C20, diodes CR15 and CR16, and resistors R132, R136, R137, R134 and R135 constitute the power supply oscillator. The oscillator produces a triangular wave and negative pulses, at a frequency of 20 KHz. Comparator U34-6,7/1 compares the triangular wave with the DC control voltage (U33-9) and produces the pulses to drive the power supply switch.

Diode CR14 clamps the width of the output pulses at U34-1.

The pulses at various points of the network are illustrated in the diagram below:

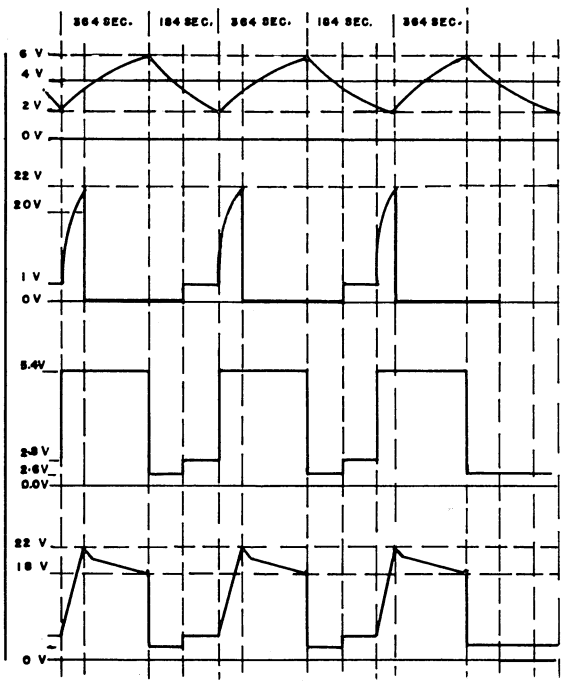


Figure 5-12. Power Supply Signals

The transistors Q7 and Q6 together with their networks constitute the driver circuits for power transistor Q9.

U33 is the voltage regulator of the power supply. The current limit operation mode is based on the fact that the maximum current through the main branch (transistor Q9, choke T1) is the same as the maximum current which is transferred by the CR21 clamp diode circuit whenever Q9 does not conduct.

The voltage at the junction of R141/R142 is a reference parameter for the current limiter.

R139 is connected at U33-6; this reference point has an approximate voltage of 7.2 vdc. The resistor-network R138 and R139 determines the voltage at U34-10.

The input at U34-13 goes high and provides an enable at U33-2. The voltage at Vz (U33-9) drops down and the width of the output pulses become narrower, and the output voltage is reduced.

The network formed from U34-4,5/2, transistor Q8, SCR, diodes CR17-CR40, together with resistors and capacitors provides overvoltage protection. Whenever an overvoltage is present, the SCR shorts the secondary of the transformer and the fuse at primary will open. The switching power supply provides +5vdc at 6A.

MAINTENANCE

Preventative Maintenance

Preventative maintenance is limited to running diagnostics.

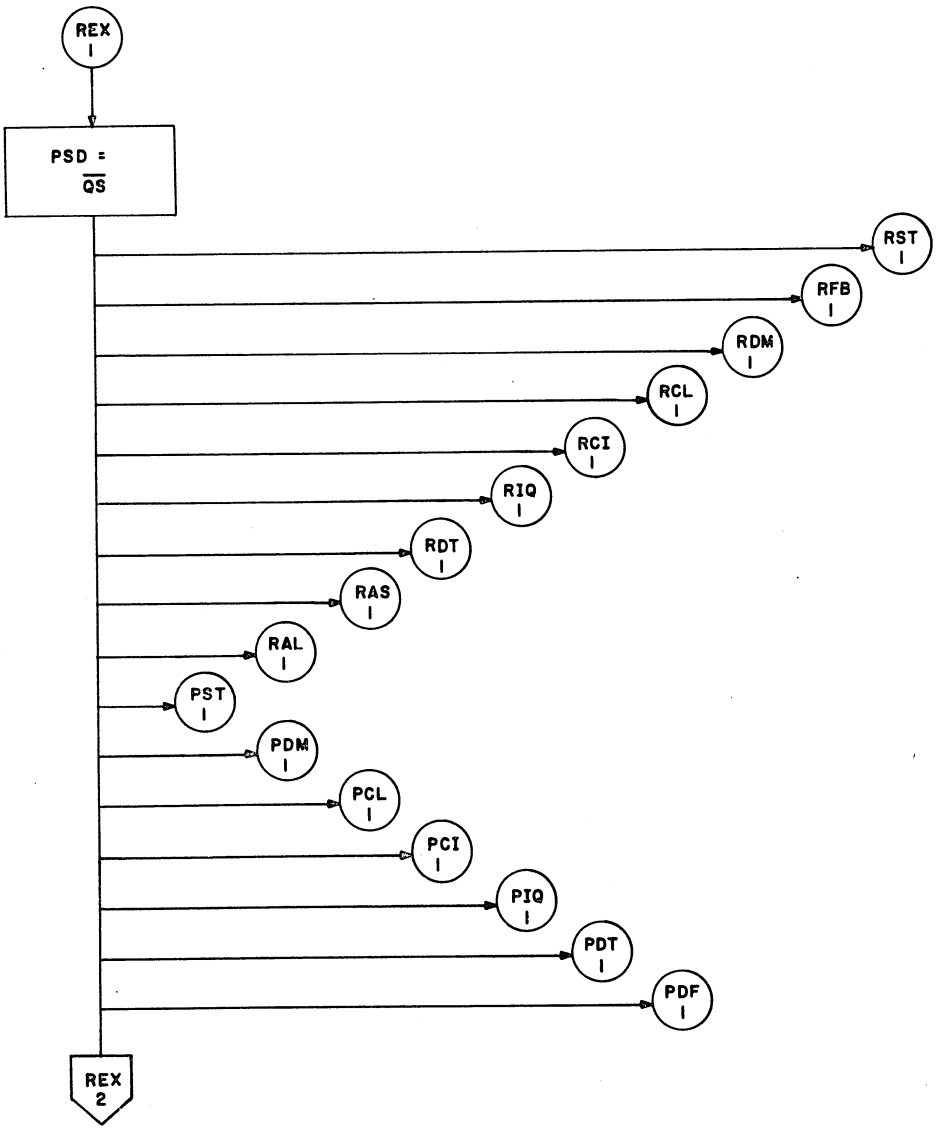
Operating Adjustments

No operating adjustments are required, except for the initial setting of the manual control jumpers.

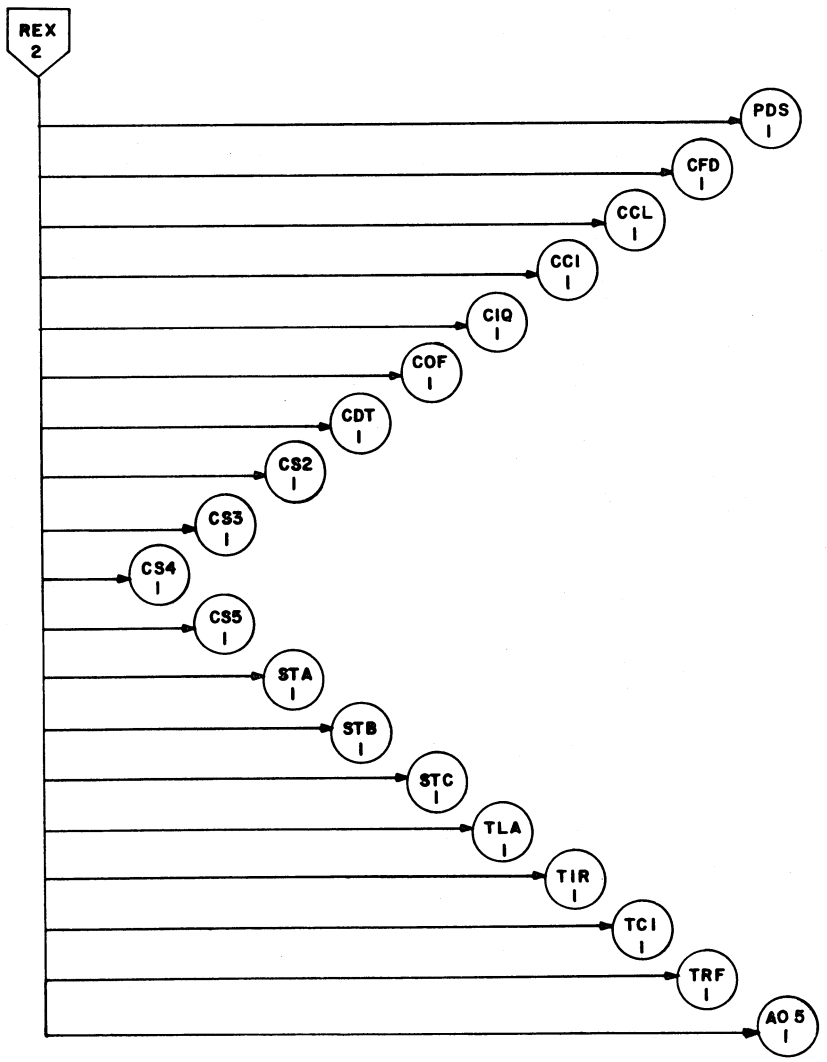
Repair

Maintenance for the PT/CP Controller is to use diagnostics requiring minimal operator intervention through the operator's panel to determine that the Controller is defective. The defective module should be replaced in the field and be taken to a depot for repair.

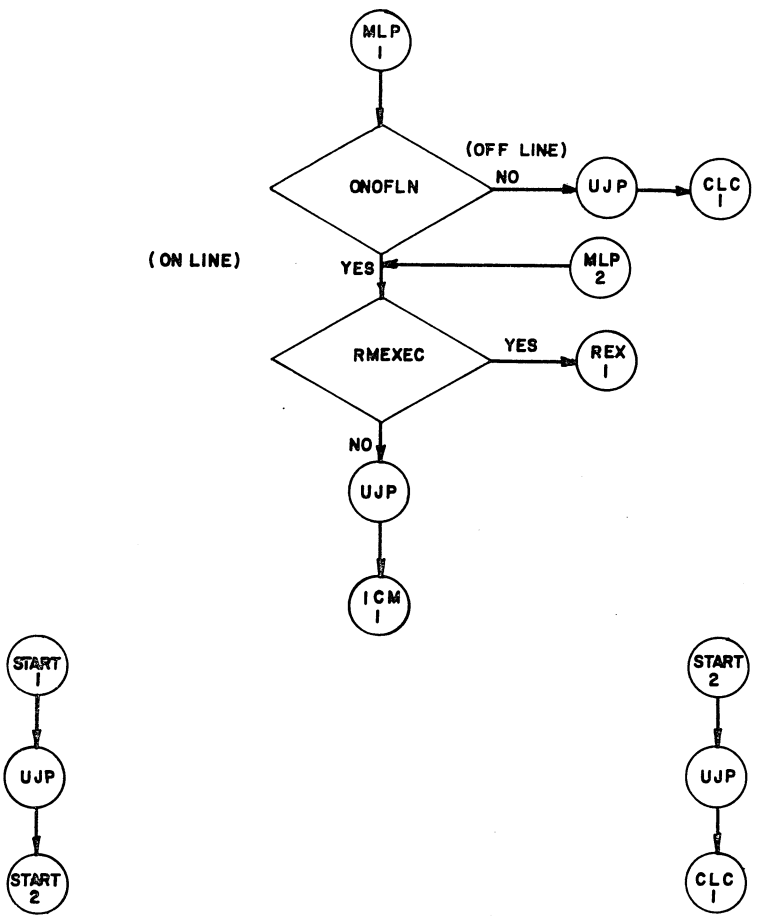
FLOW CHARTS



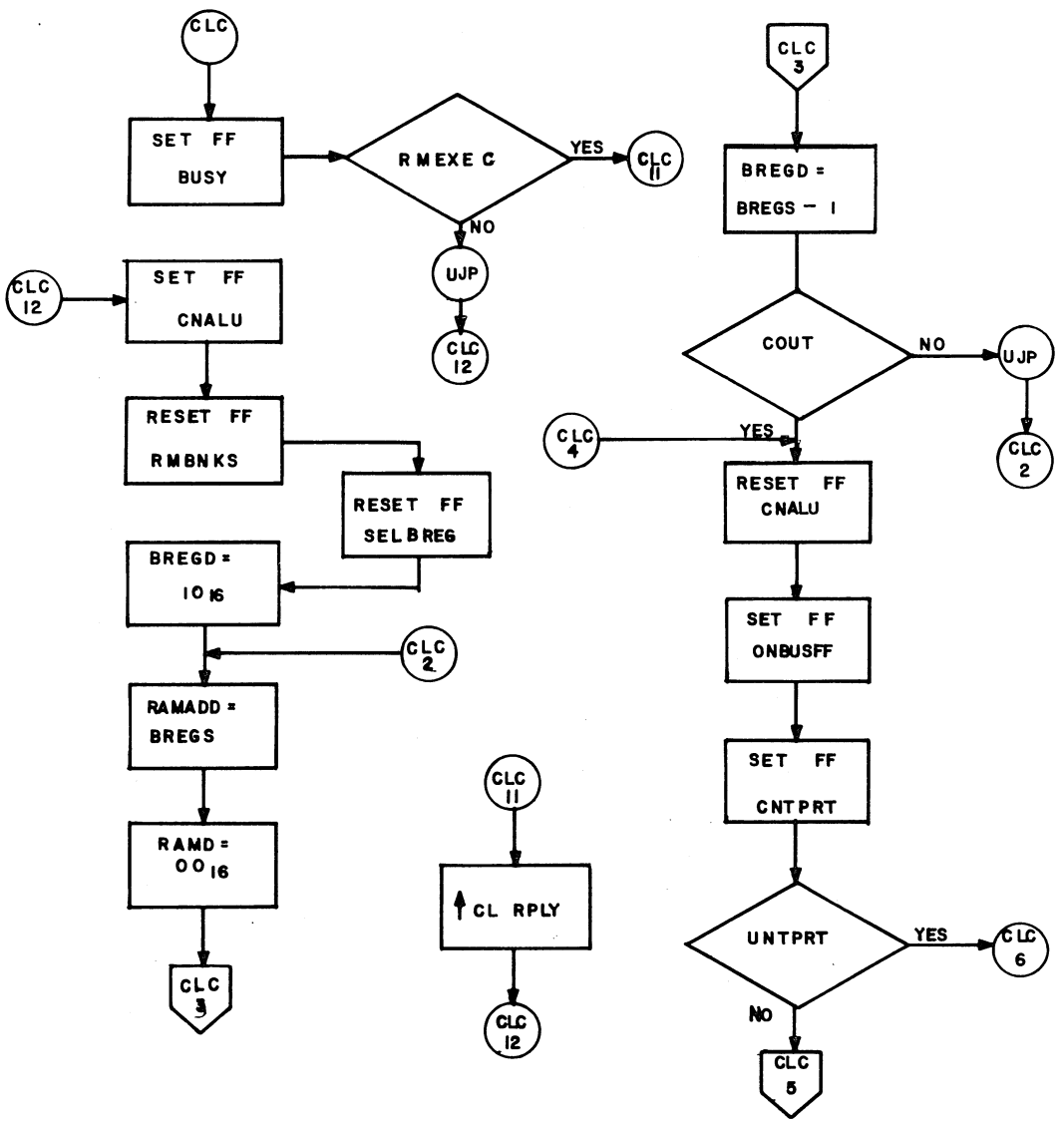
Q LINE DECODE



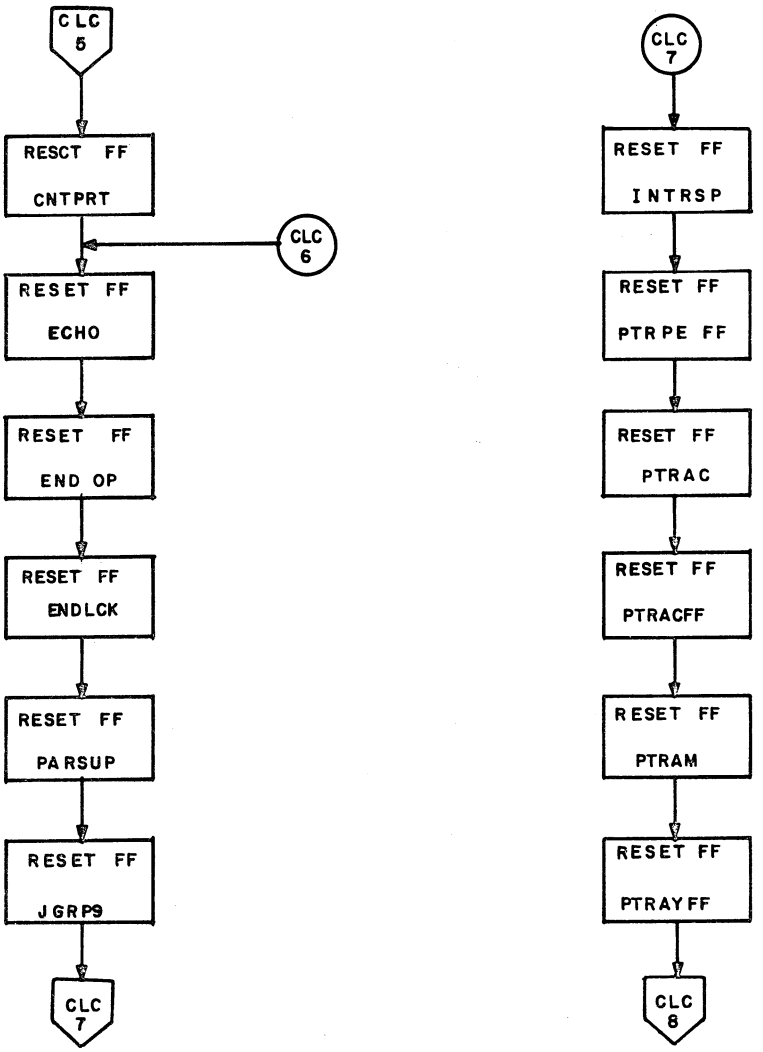
Q LINE DECODE (CONTINUED)



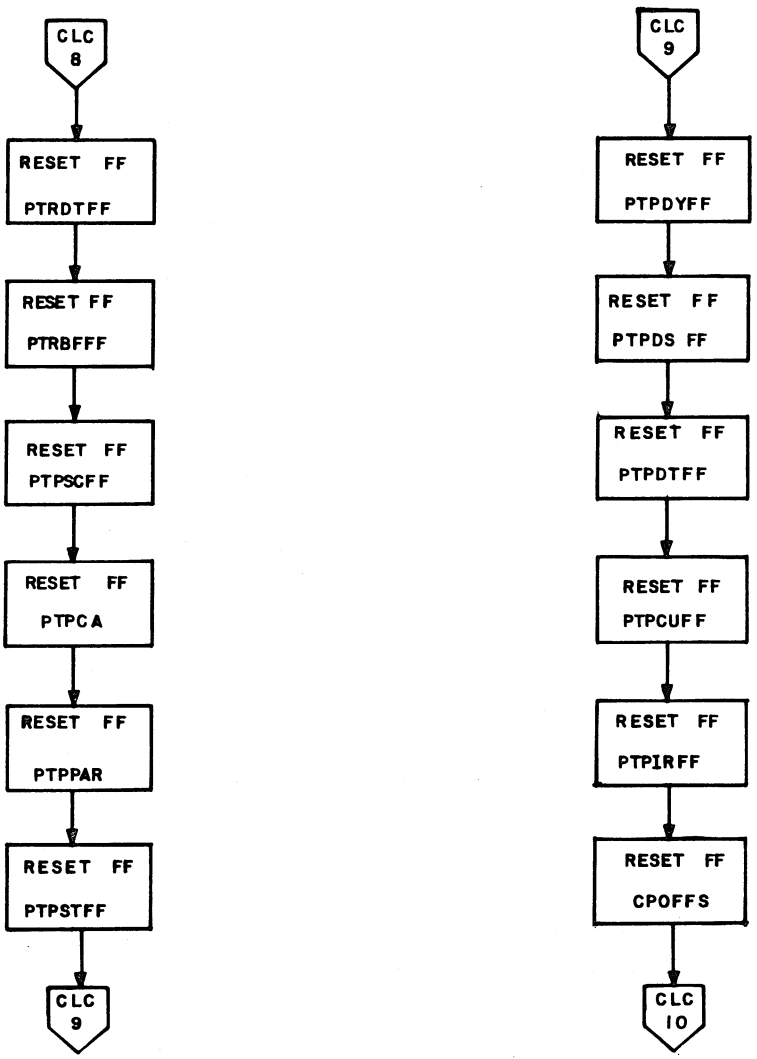
MAIN LOOP INTERNAL



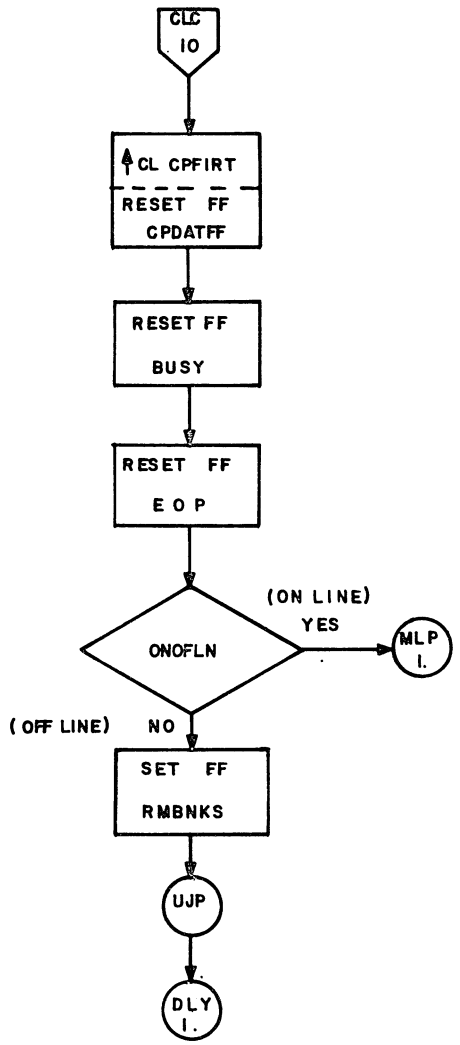
CLEAR CONTROLLER A/Q & INTERRUPT



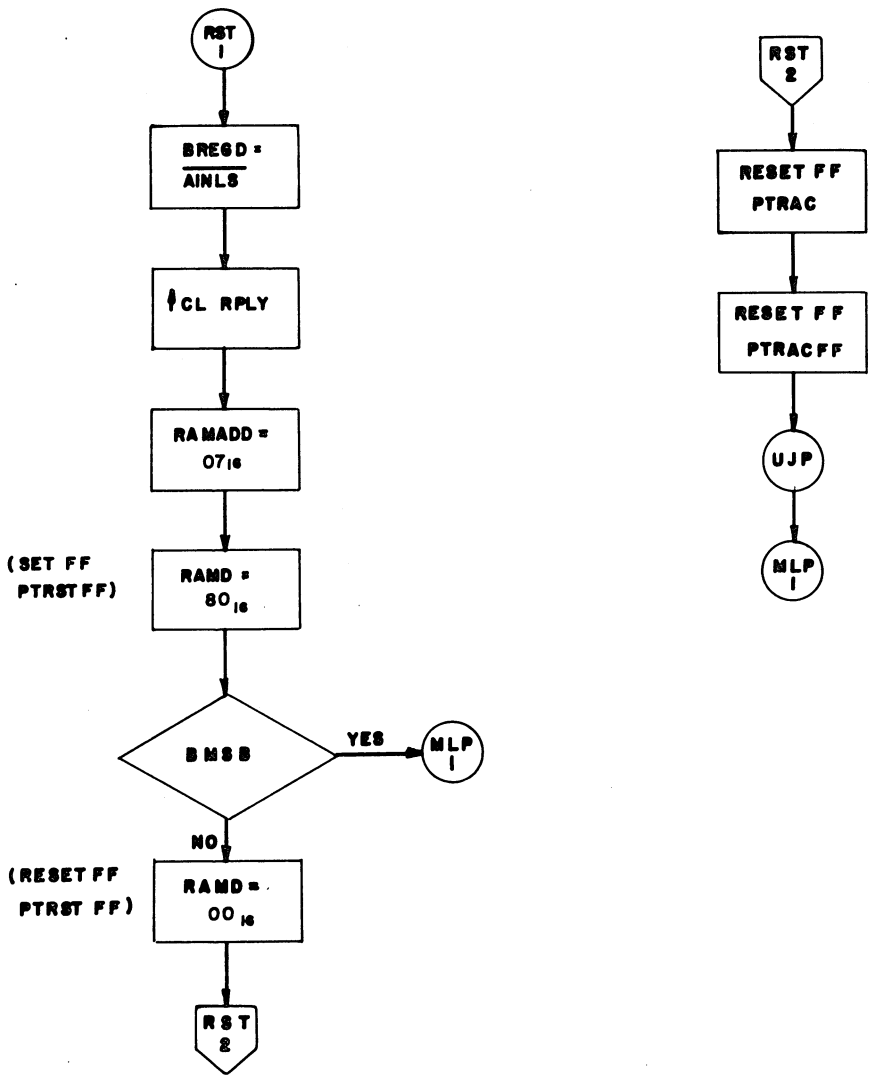
CLEAR CONTROLLER A/Q & INTERRUPT (CONTINUED)



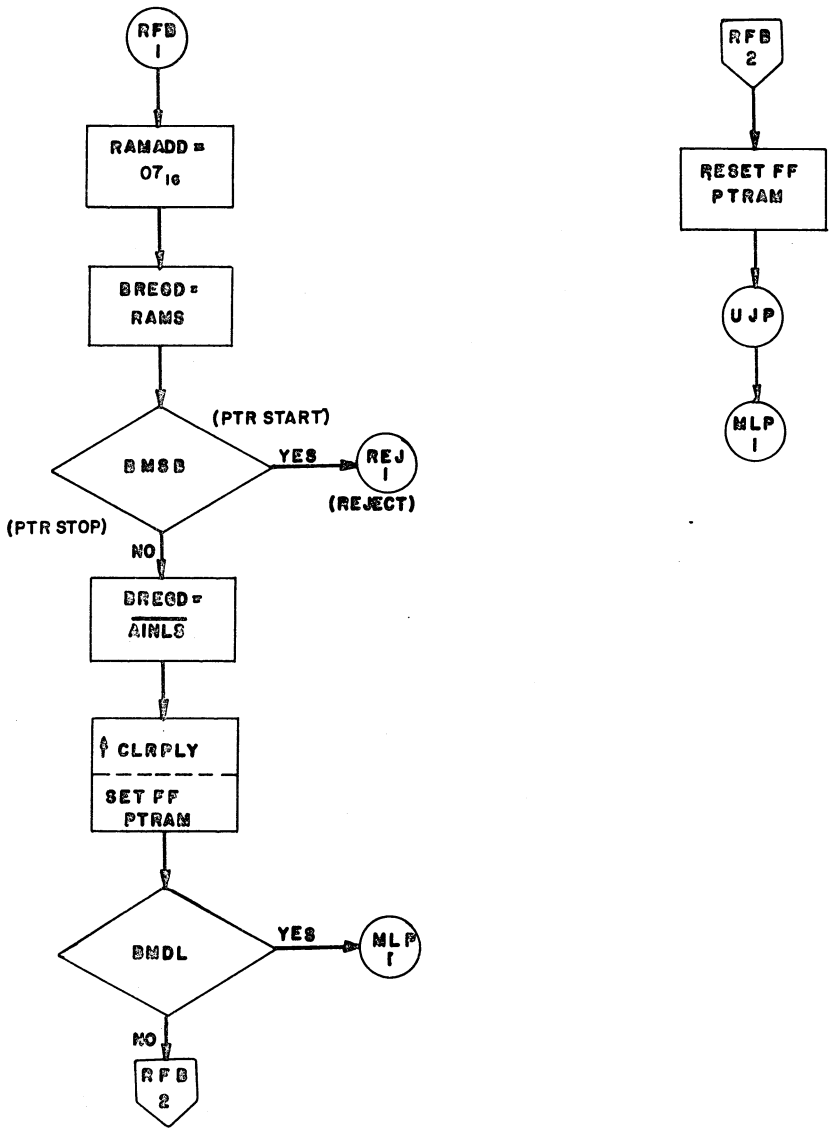
CLEAR CONTROLLER A/Q & INTERRUPT (CONTINUED)



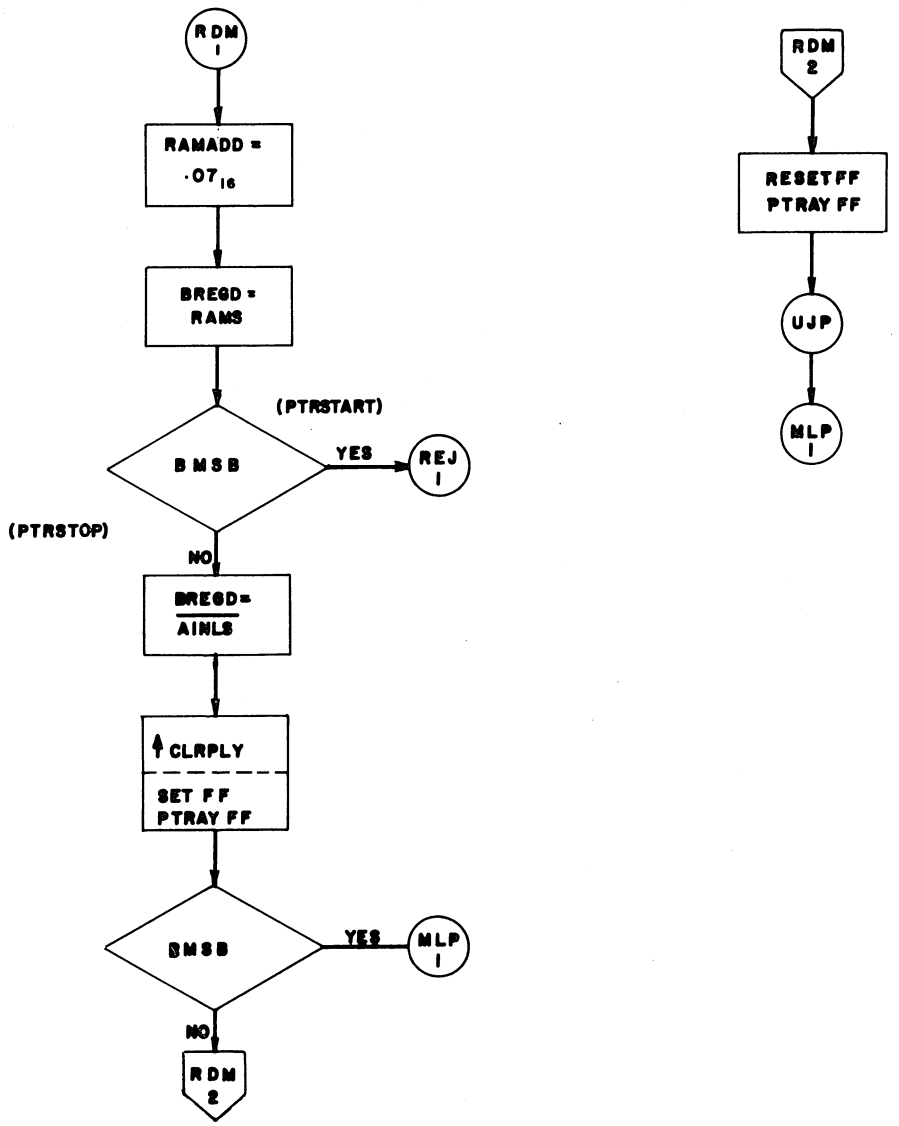
CLEAR CONTROLLER A/Q & INTERRUPT (CONTINUED)



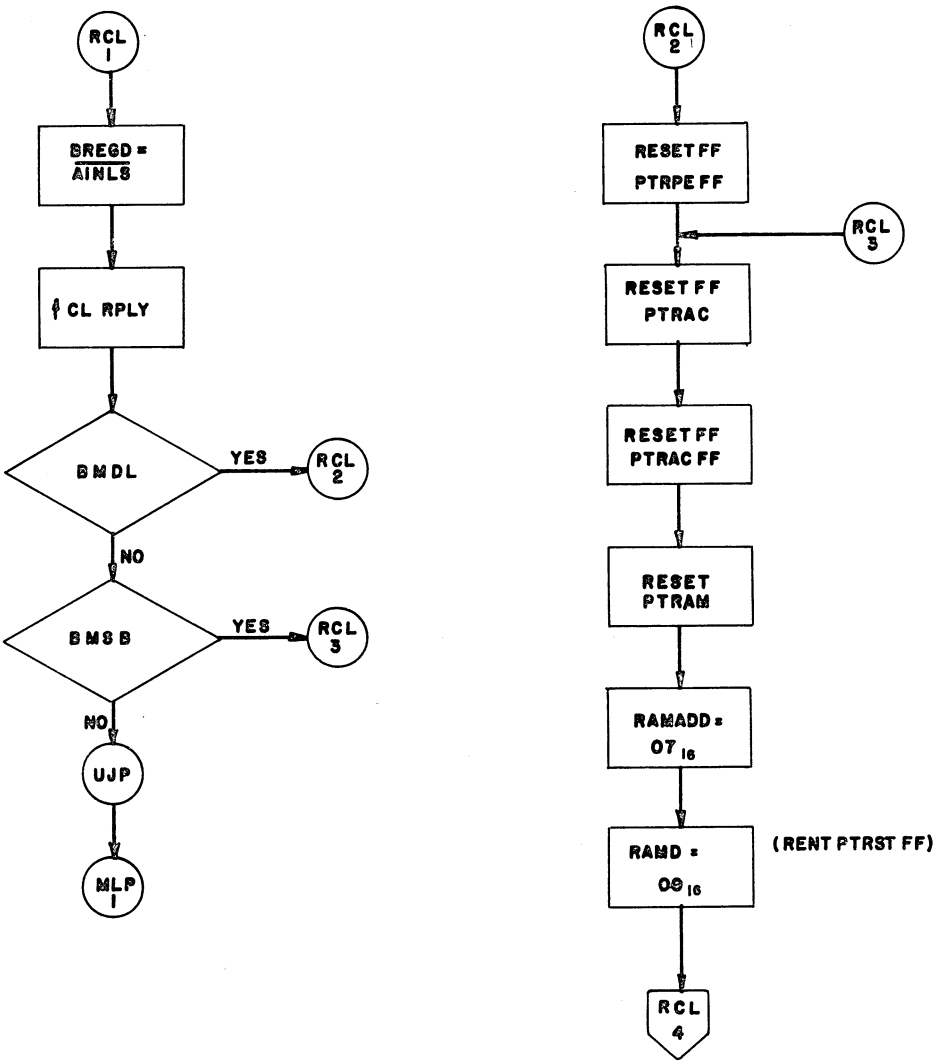
PTR STOP-START A/Q COMMAND



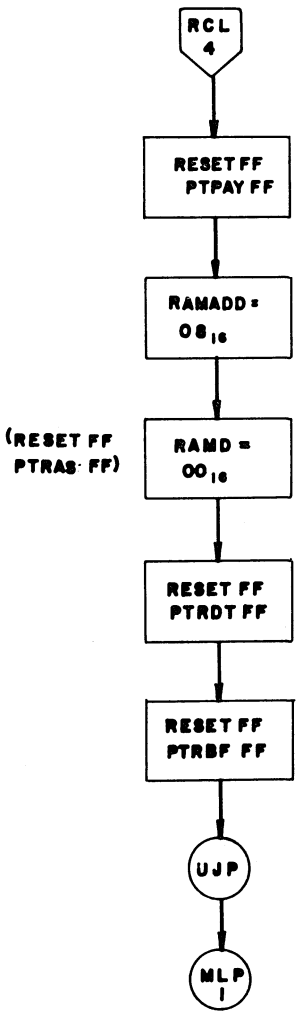
PTR FORWARD-BACKWARD A/Q COMMAND



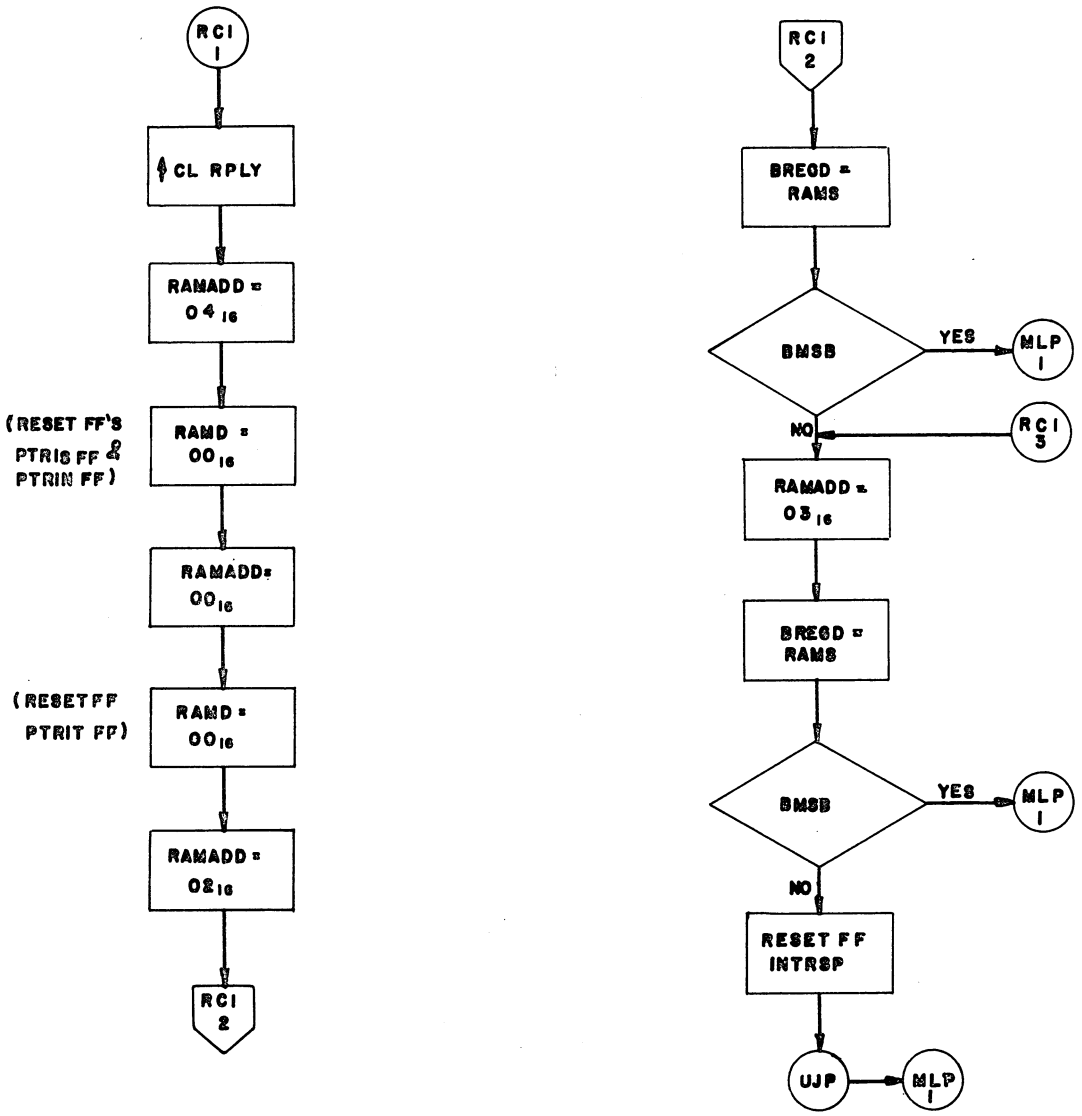
PTR DATA MODE A/Q COMMAND



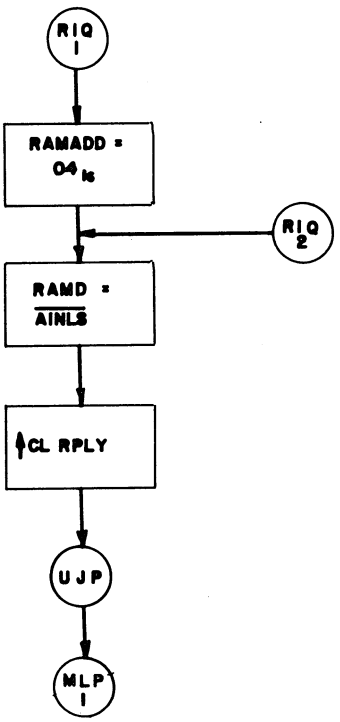
PTR CLEAR A/Q COMMAND



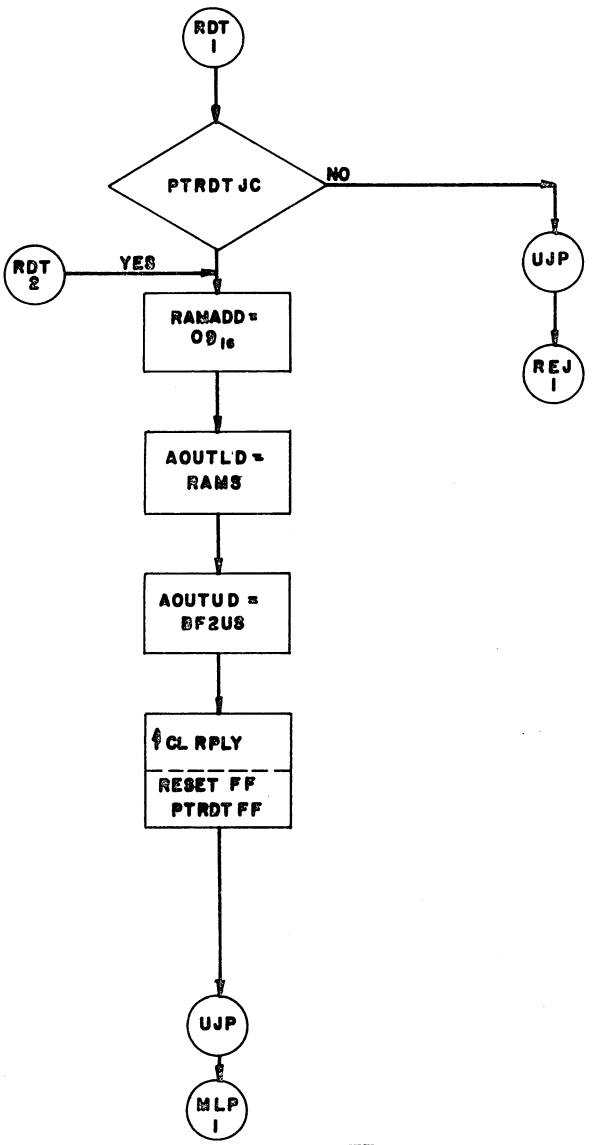
PTR CLEAR A/Q (CONTINUED)



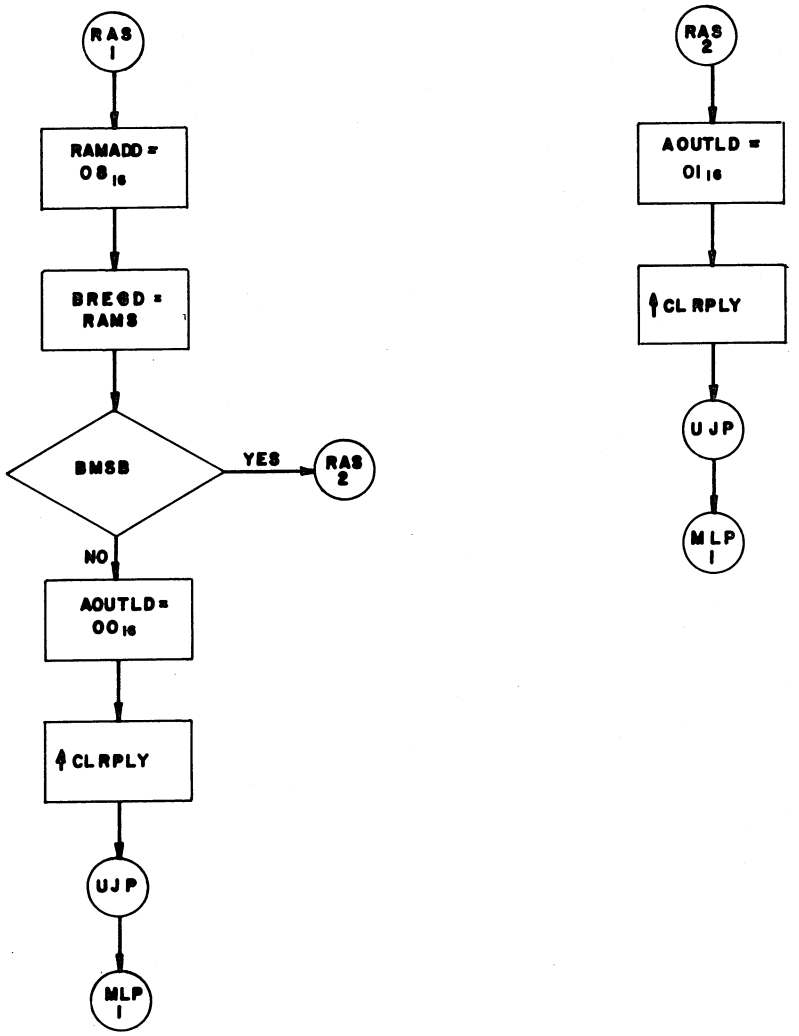
PTR CLEAR INTERRUPT A/Q COMMAND



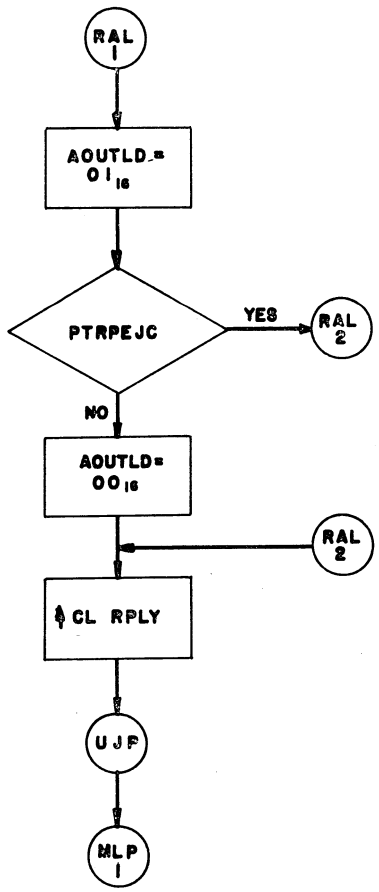
PTR INTERRUPT REQUEST A/Q COMMAND



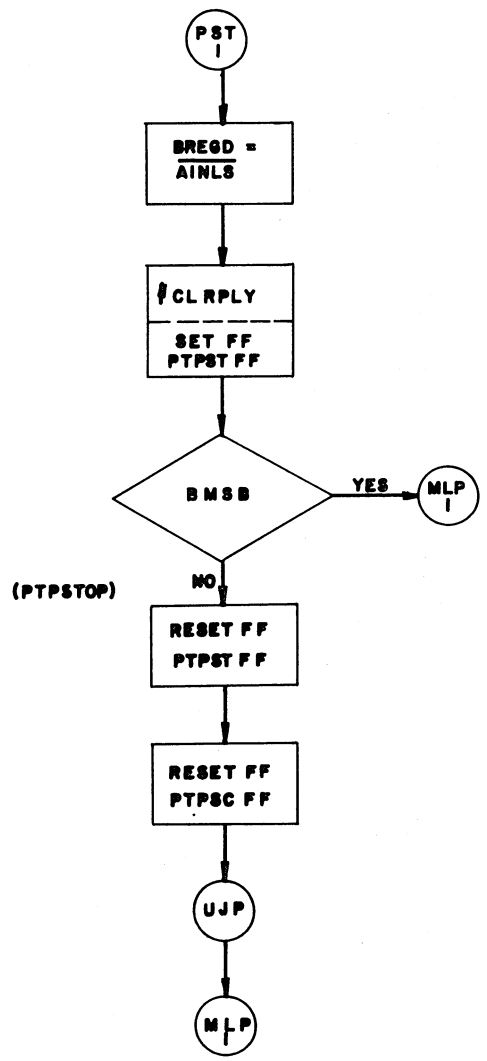
PTR READ DATA A/Q COMMAND



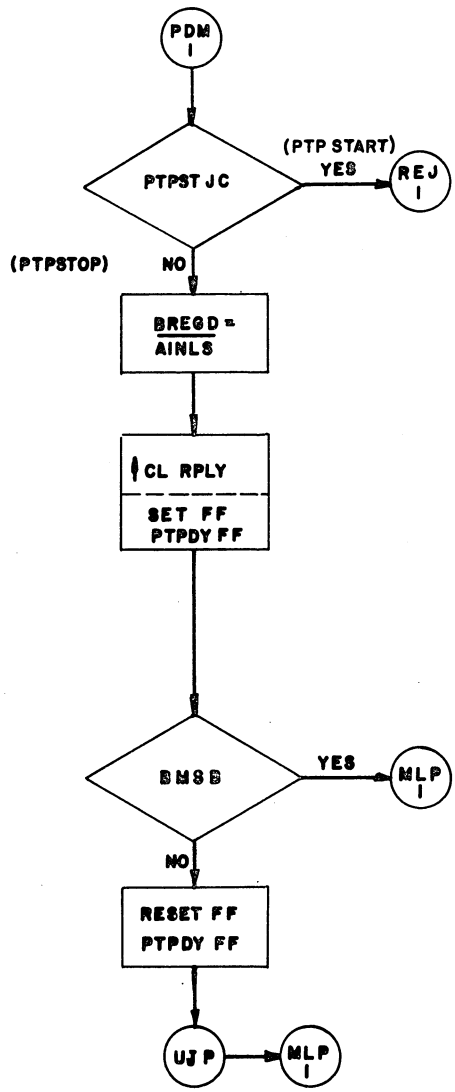
PTR ASSY TRANSFER STATUS A/Q COMMAND



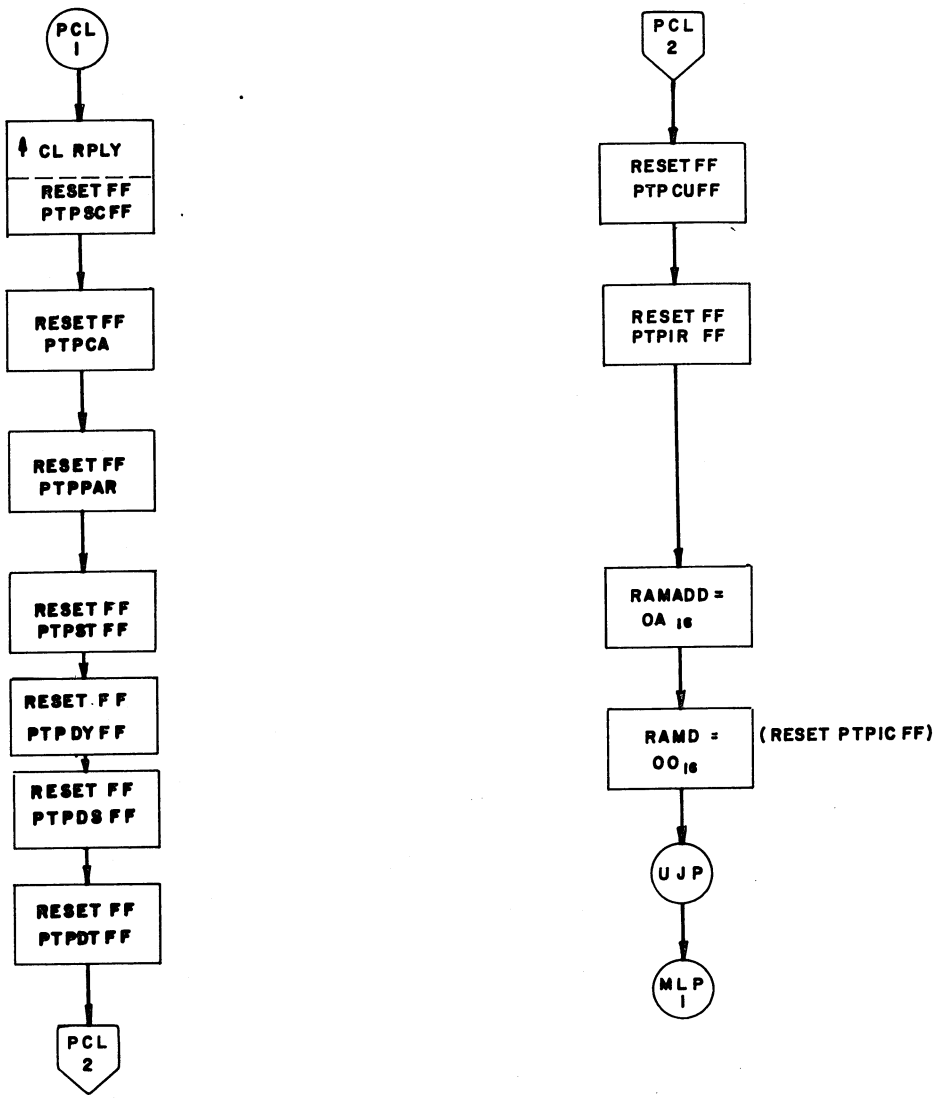
PTR ALARM STATUS A/Q COMMAND



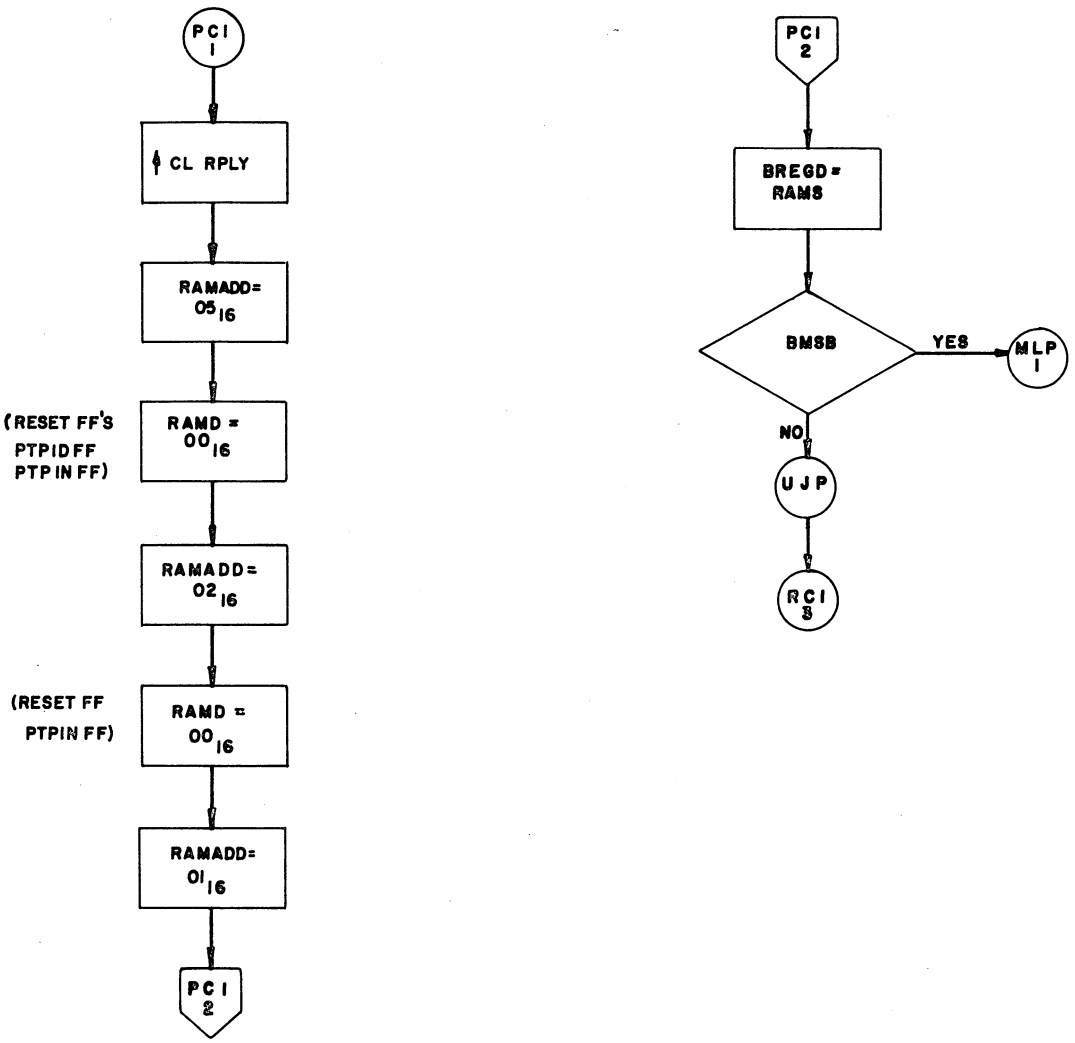
PTP STOP-START A/Q COMMAND



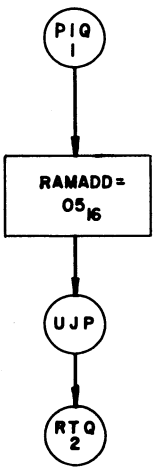
PTP DATA MODE A/Q COMMAND



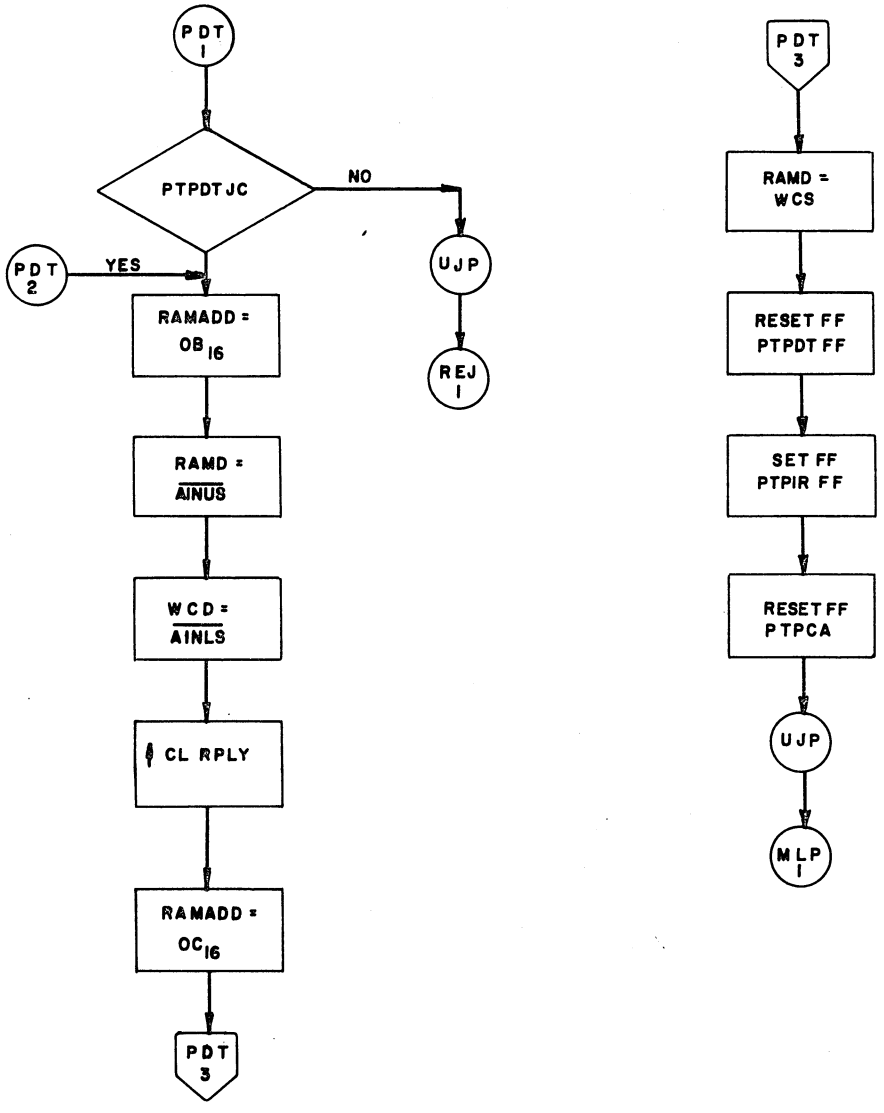
PTP CLEAR A/Q COMMAND



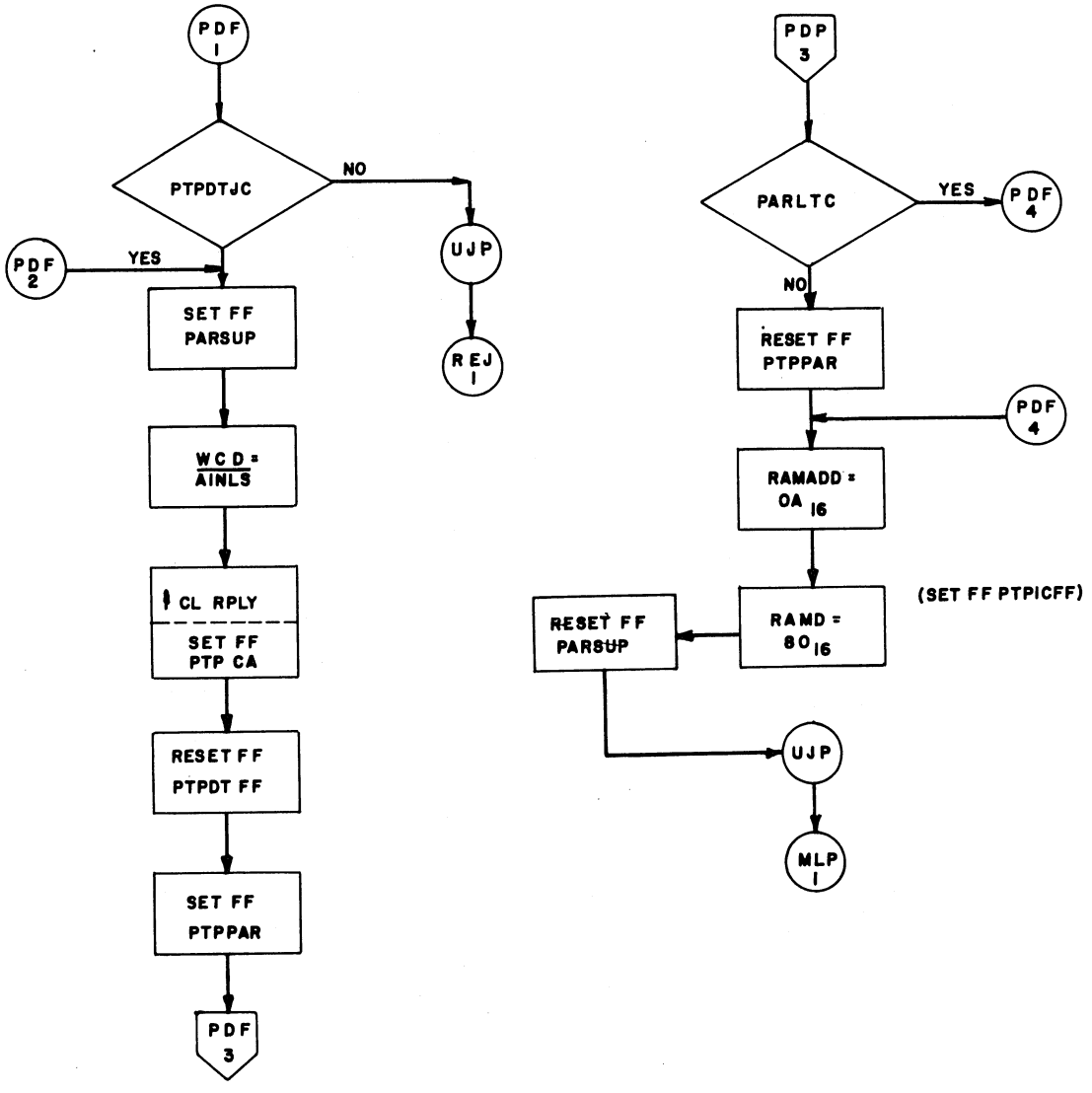
PTP CLEAR INTERRUPT A/Q COMMAND



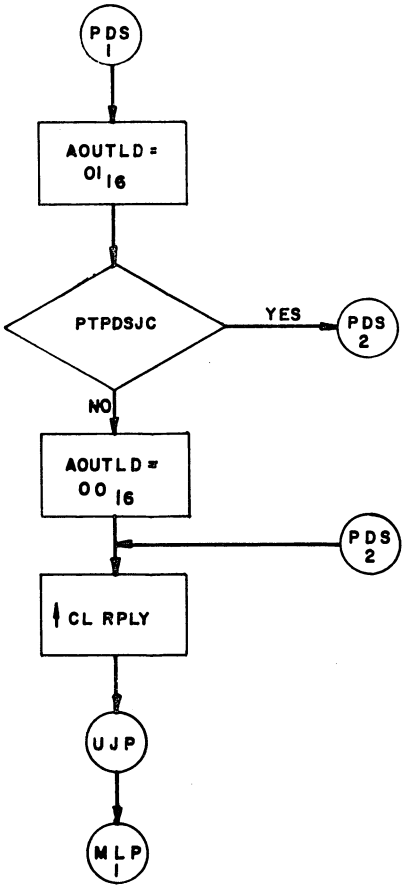
PTP INERRUPT REQUEST A/Q COMMAND



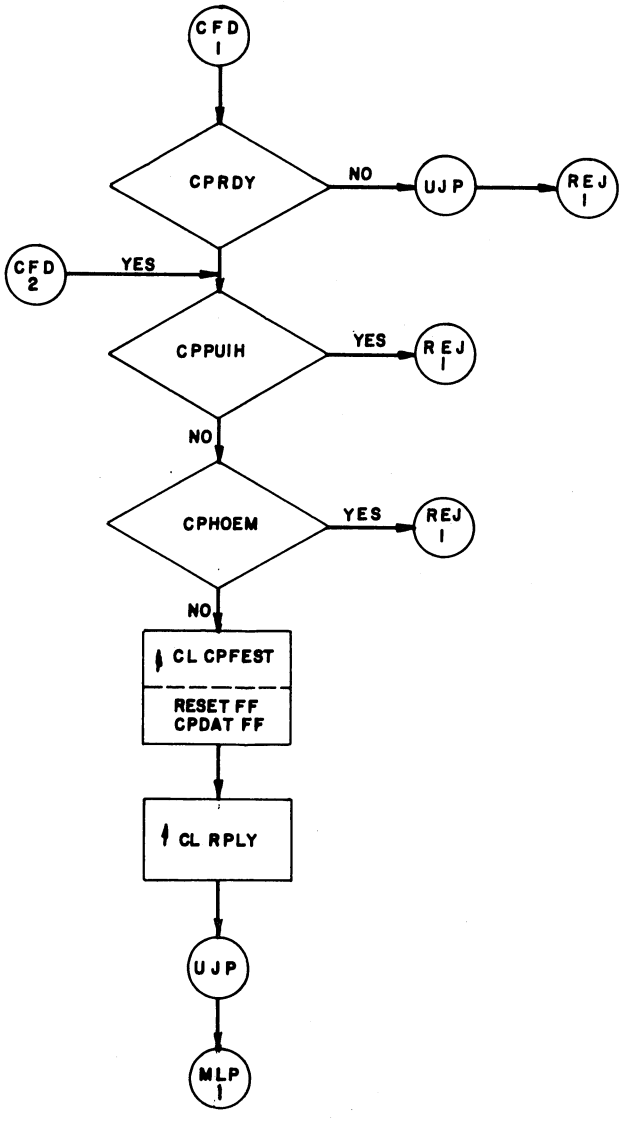
PTP DATA A/Q COMMAND



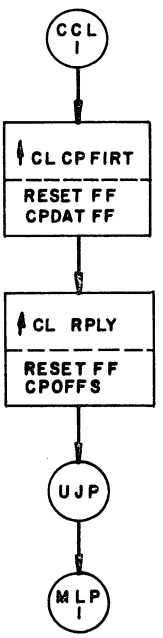
PTP DEVICE FUNCTION A/Q COMMAND



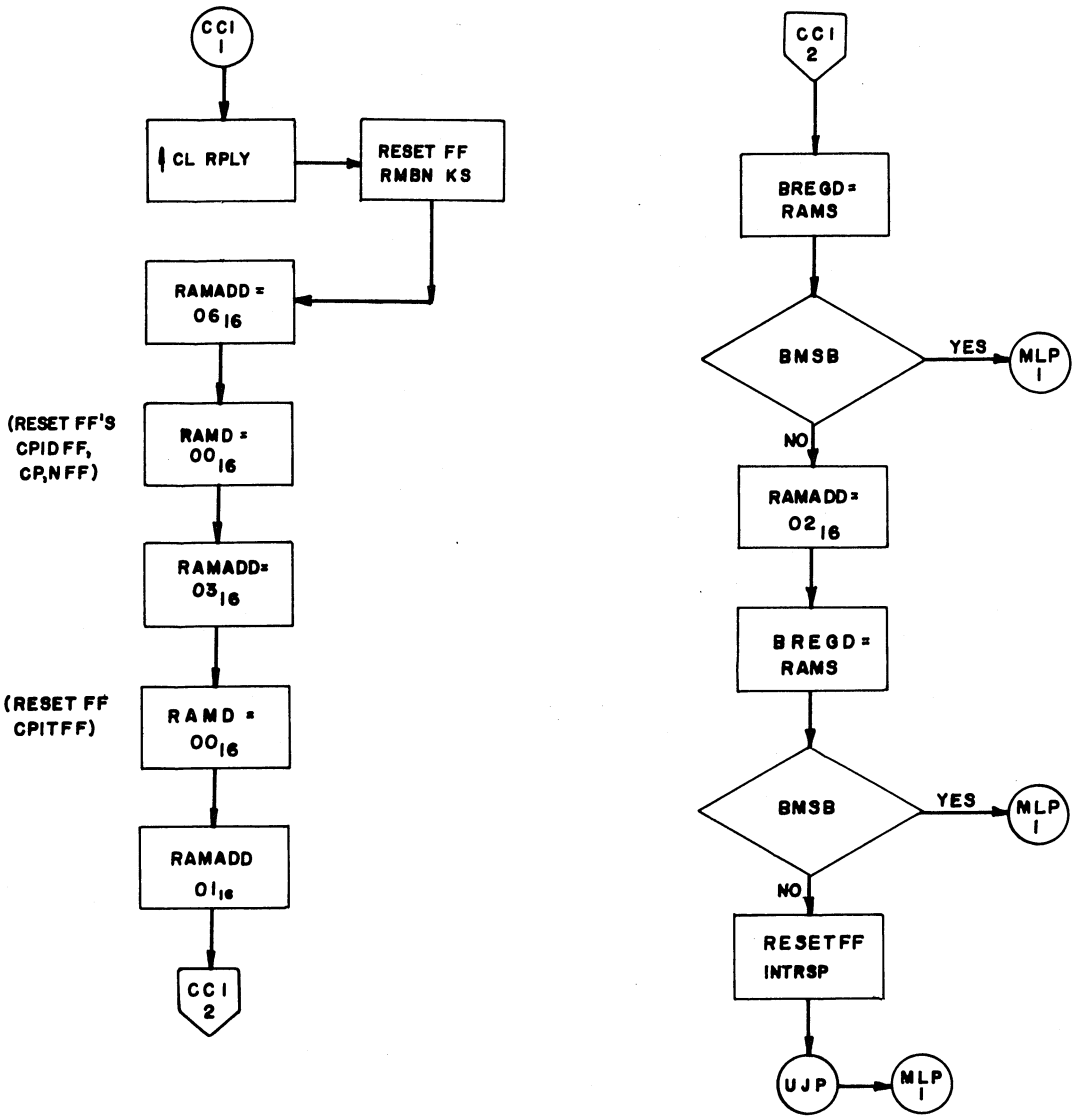
PTP DISASSEMBLY TRANSFER STATUS A/Q Command



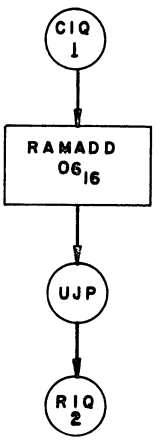
CP FEED A/Q COMMAND



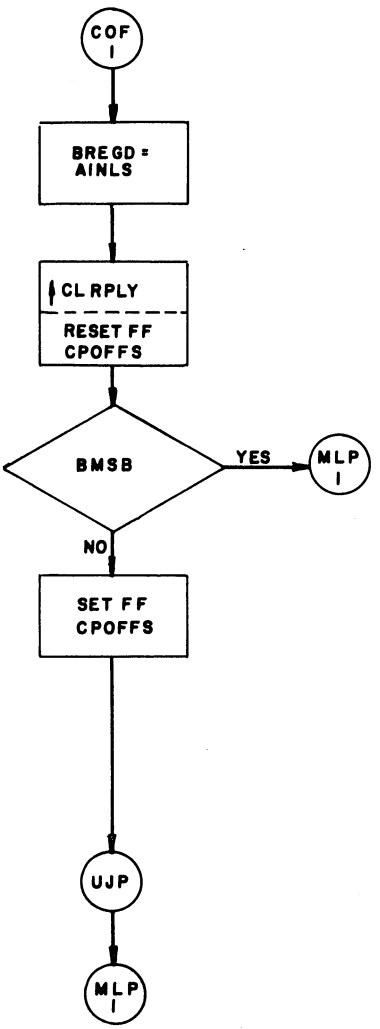
CP CLEAR A/Q COMMAND



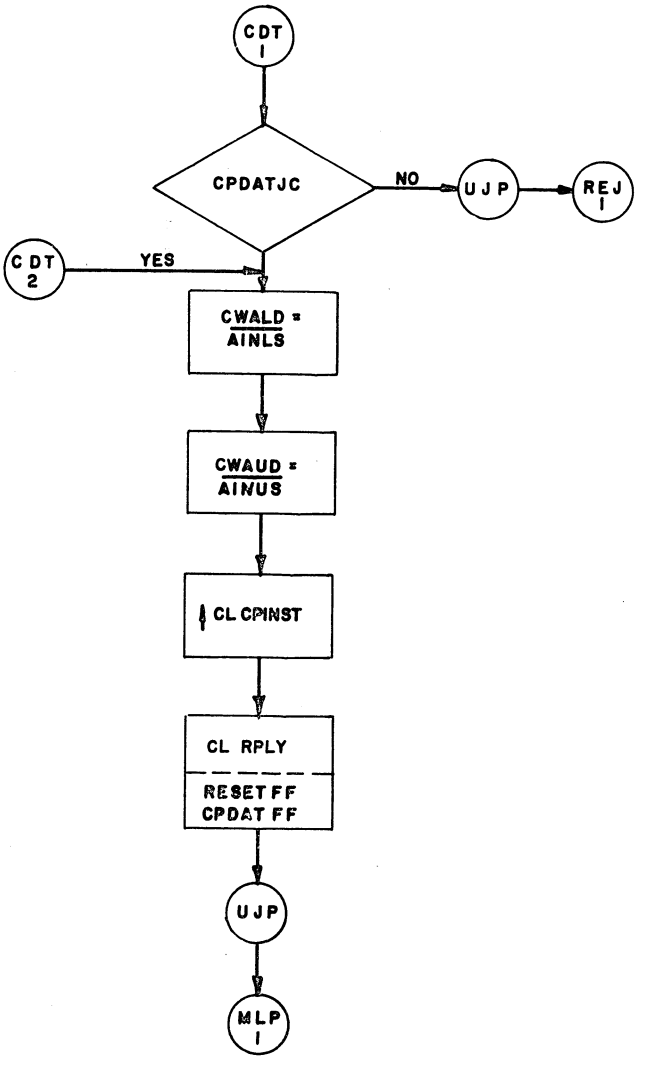
CP CLEAR INTERRUPT A/Q COMMAND



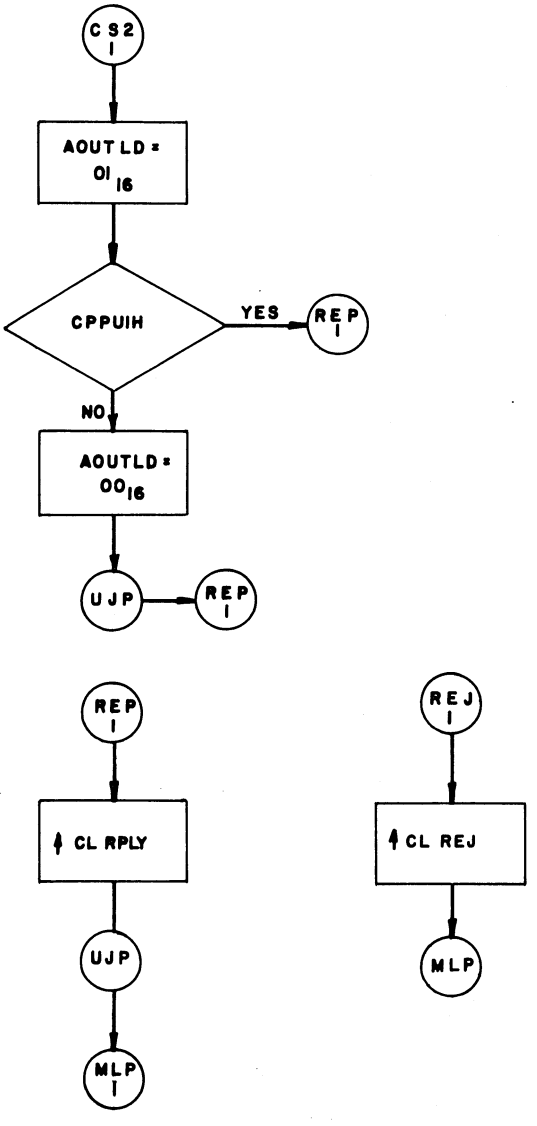
CP INTERRUPT REQUEST A/Q COMMAND



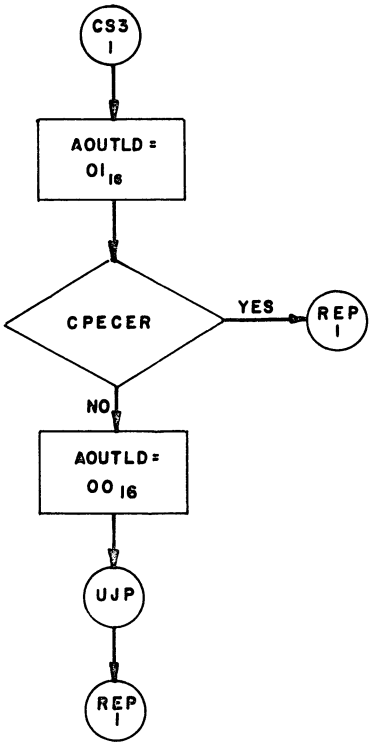
CO OFFSET A/Q COMMAND



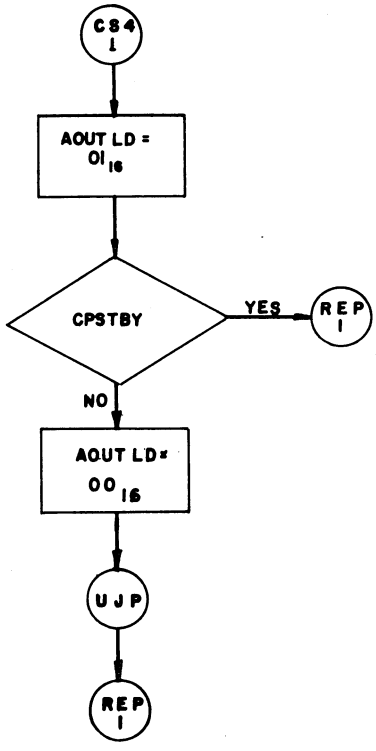
CP DATA A/Q COMMAND



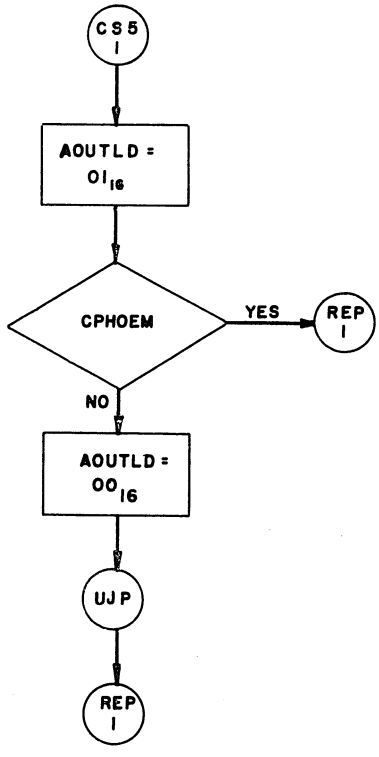
CP STATUS A/Q COMMAND



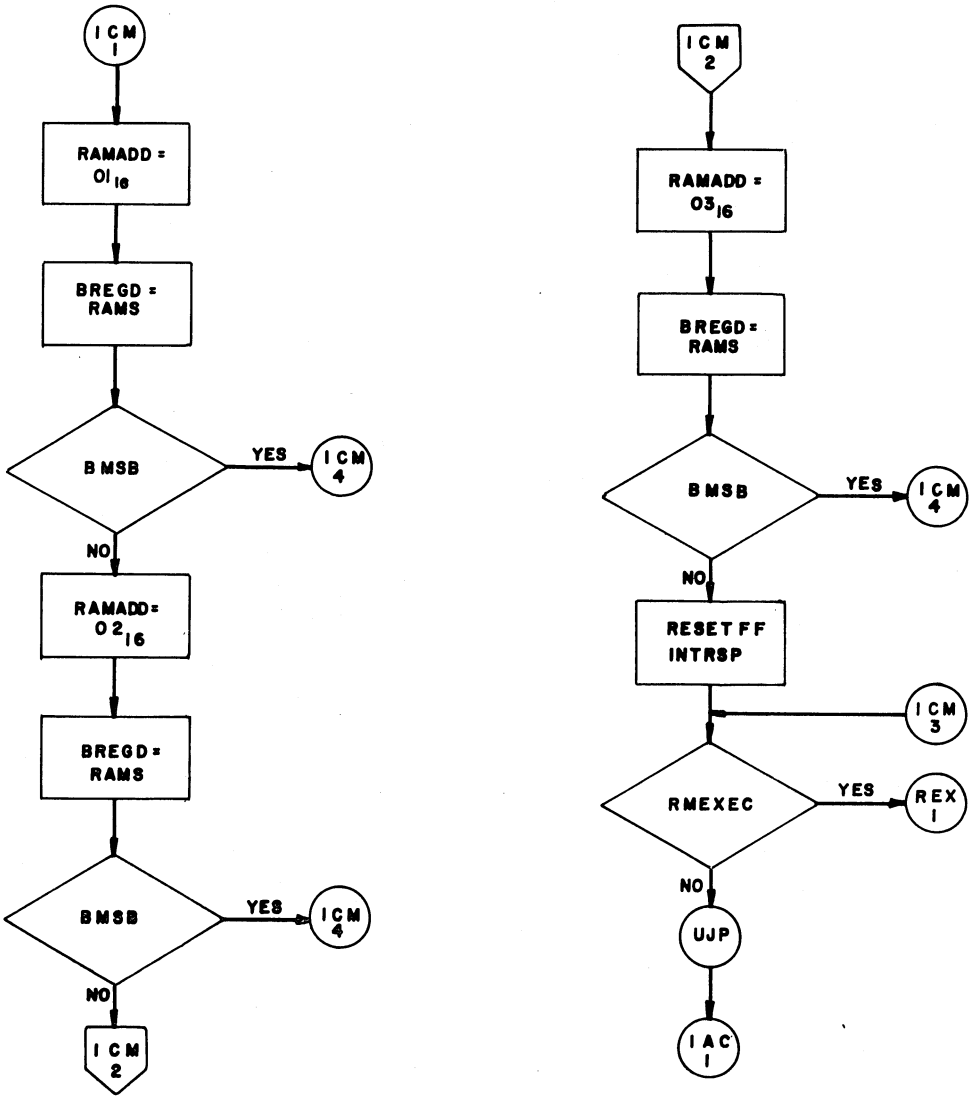
CP STATUS 3 A/Q COMMAND



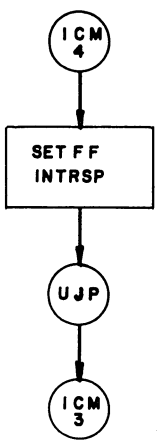
CP STATUS 4 A/Q COMMAND



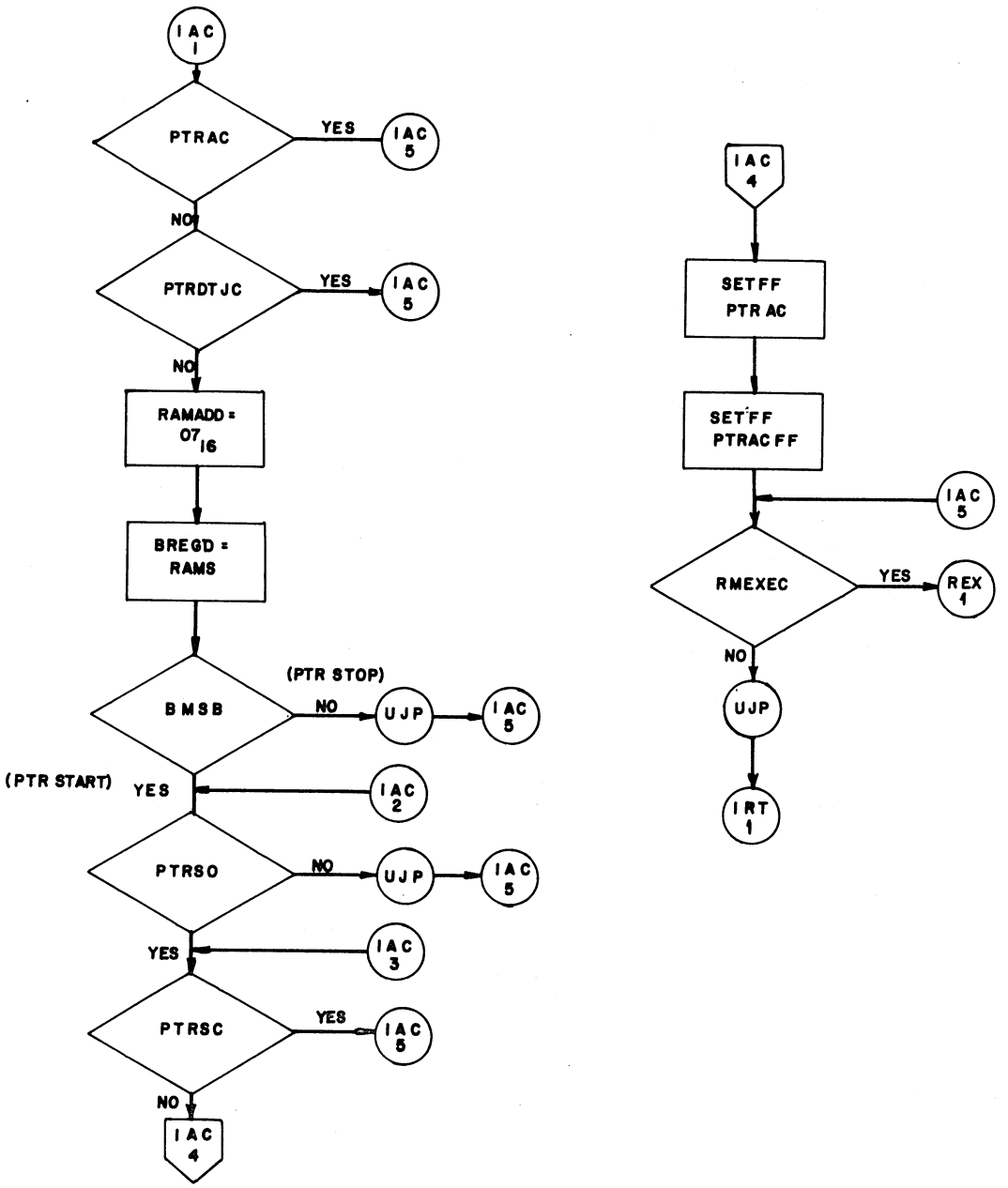
CP STATUS 5 A/Q COMMAND



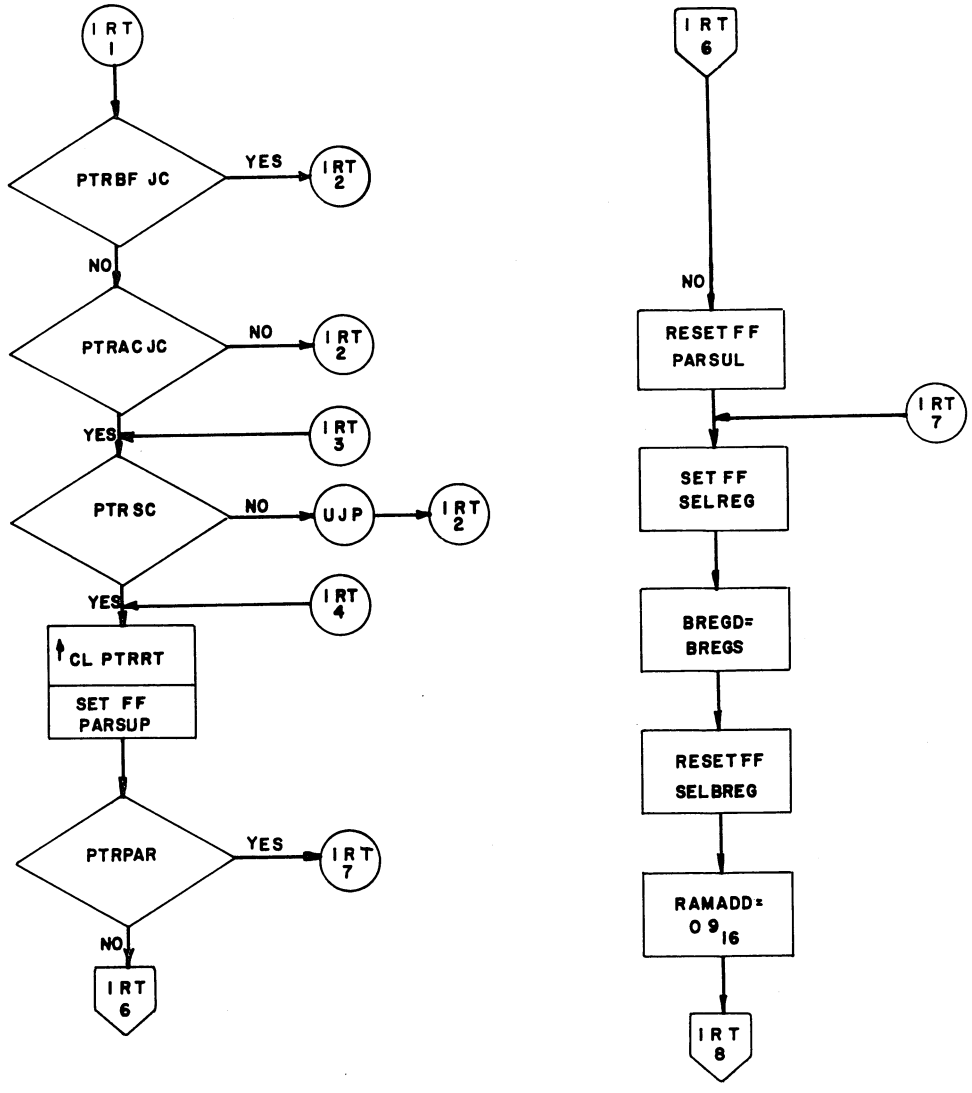
COMMON INTERRUPT, INTERVAL



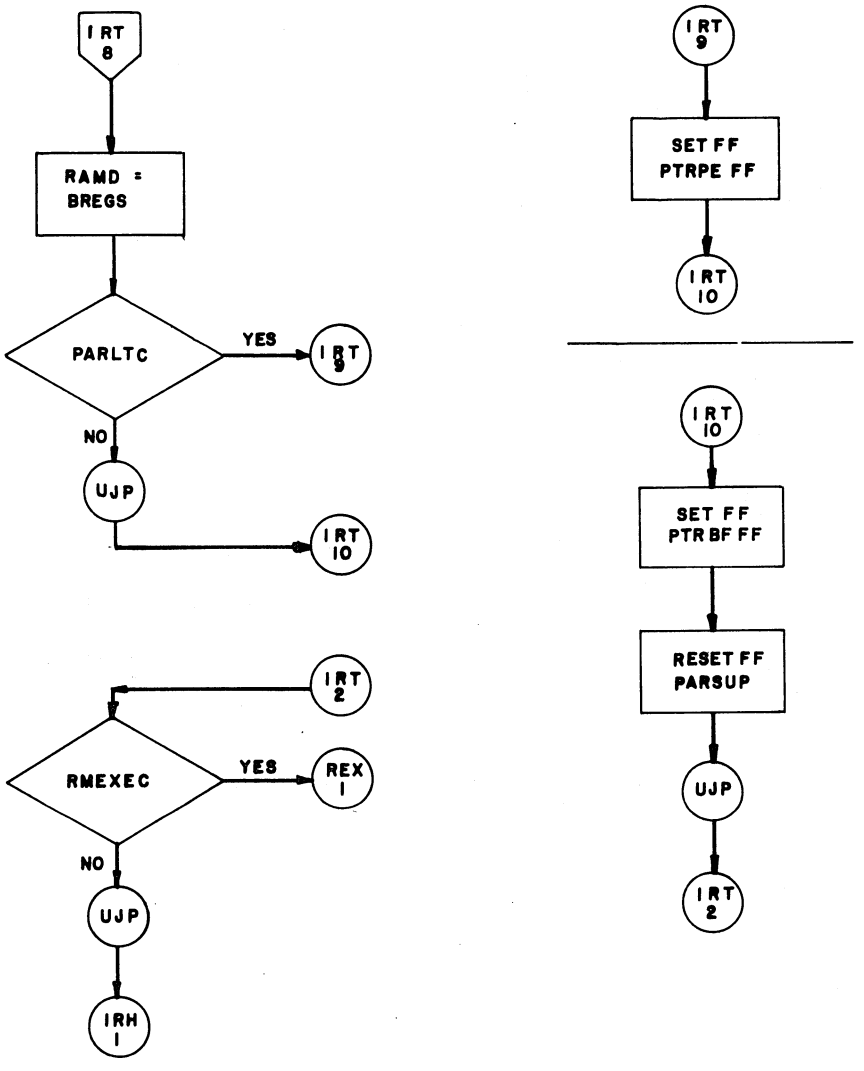
COMMON INTERRUPT, INTERVAL (Continued)



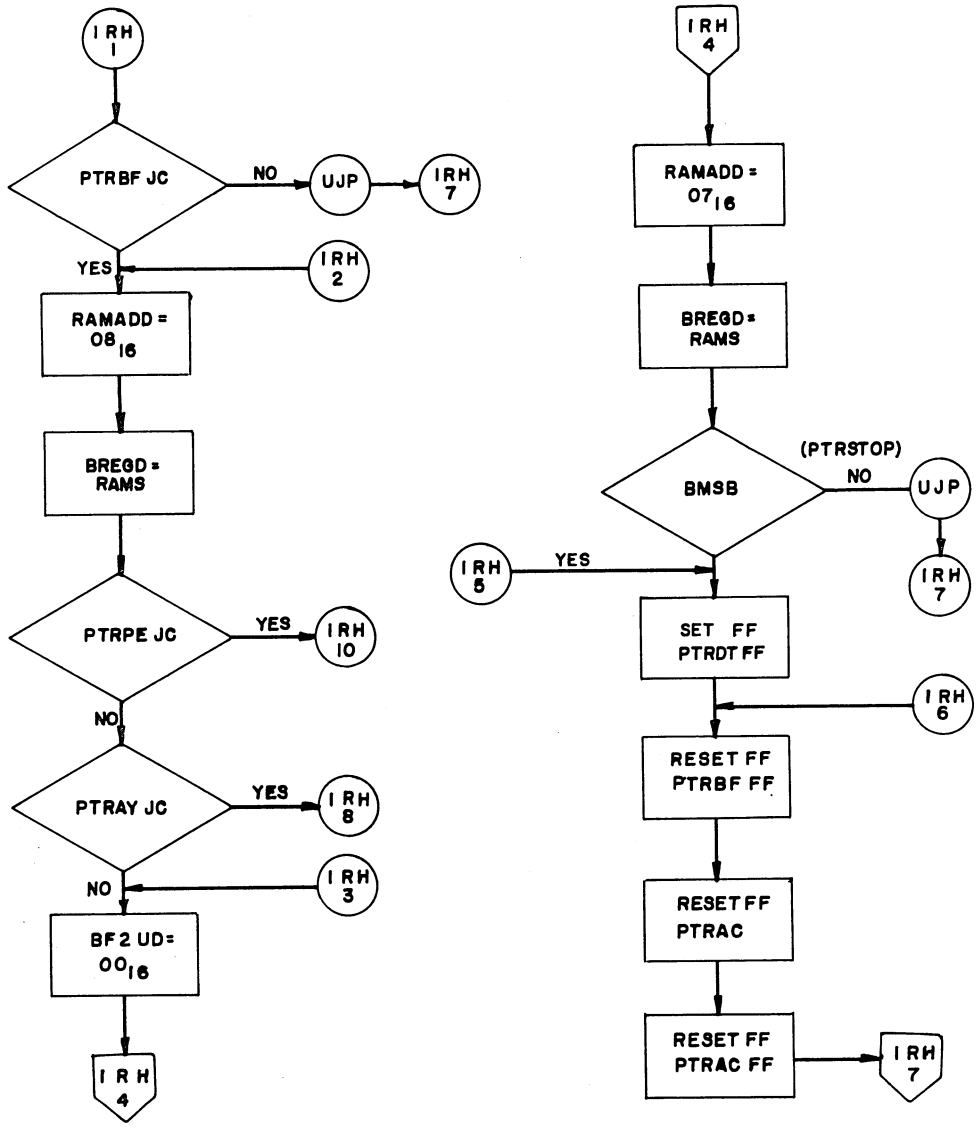
SET PTR AC, INTERNAL



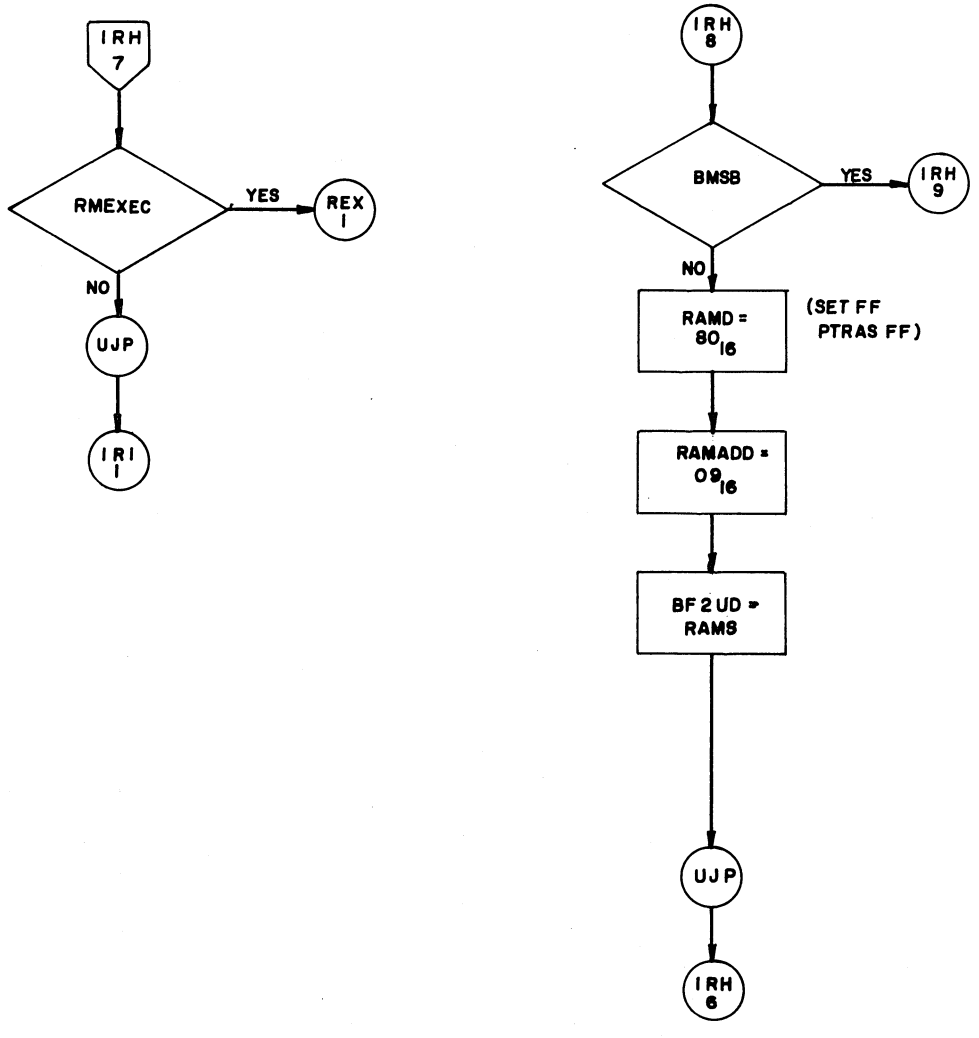
PTR CHARACTER TRANSFER, INTERNAL



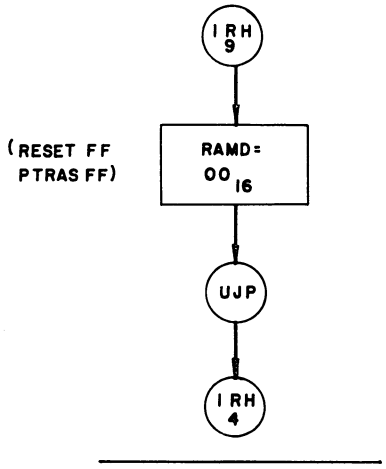
PTR CHARACTER TRANSFER (CONTINUED)

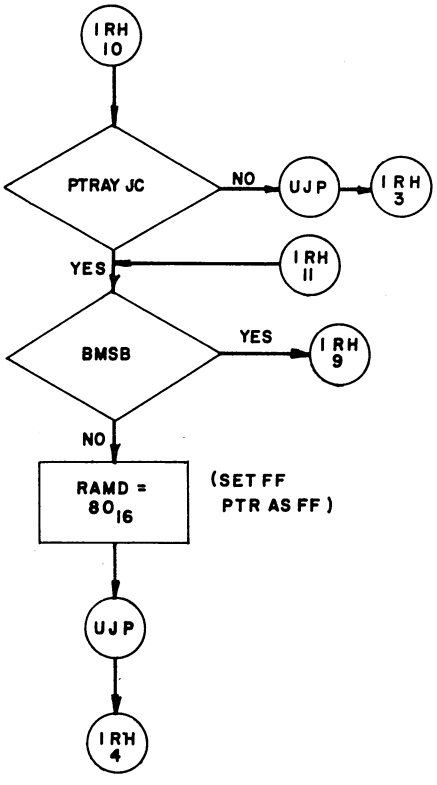


PTR CHARACTER HANDLING, INTERNAL

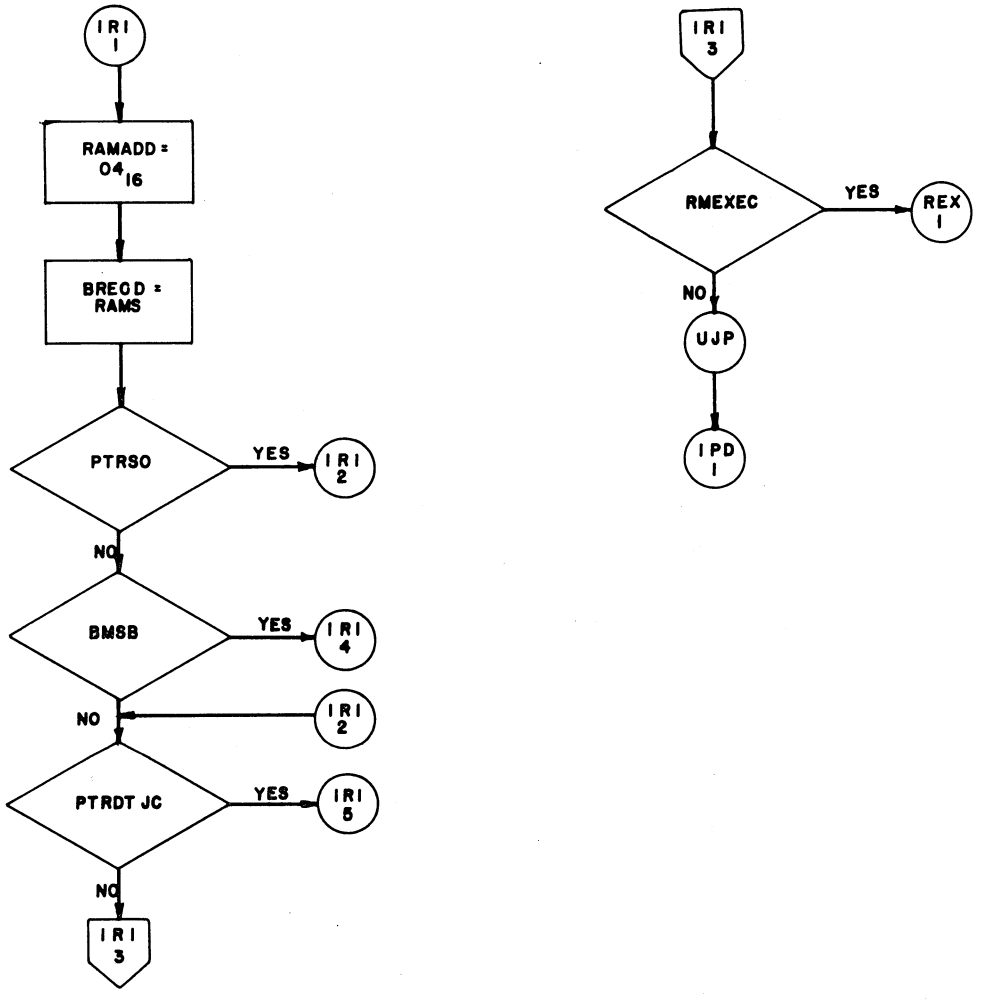


PTR CHARACTER HANDLING (CONTINUED)

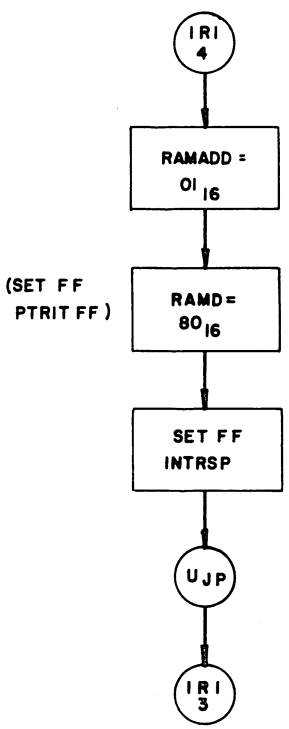


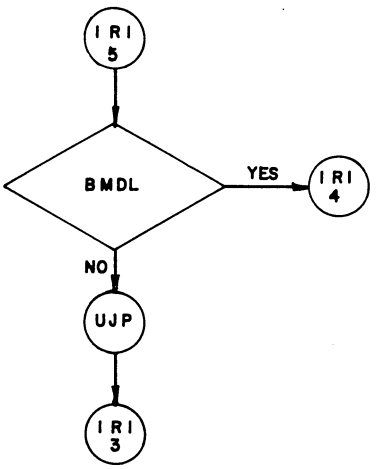


PTR CHARACTER HANDLING (CONTINUED)

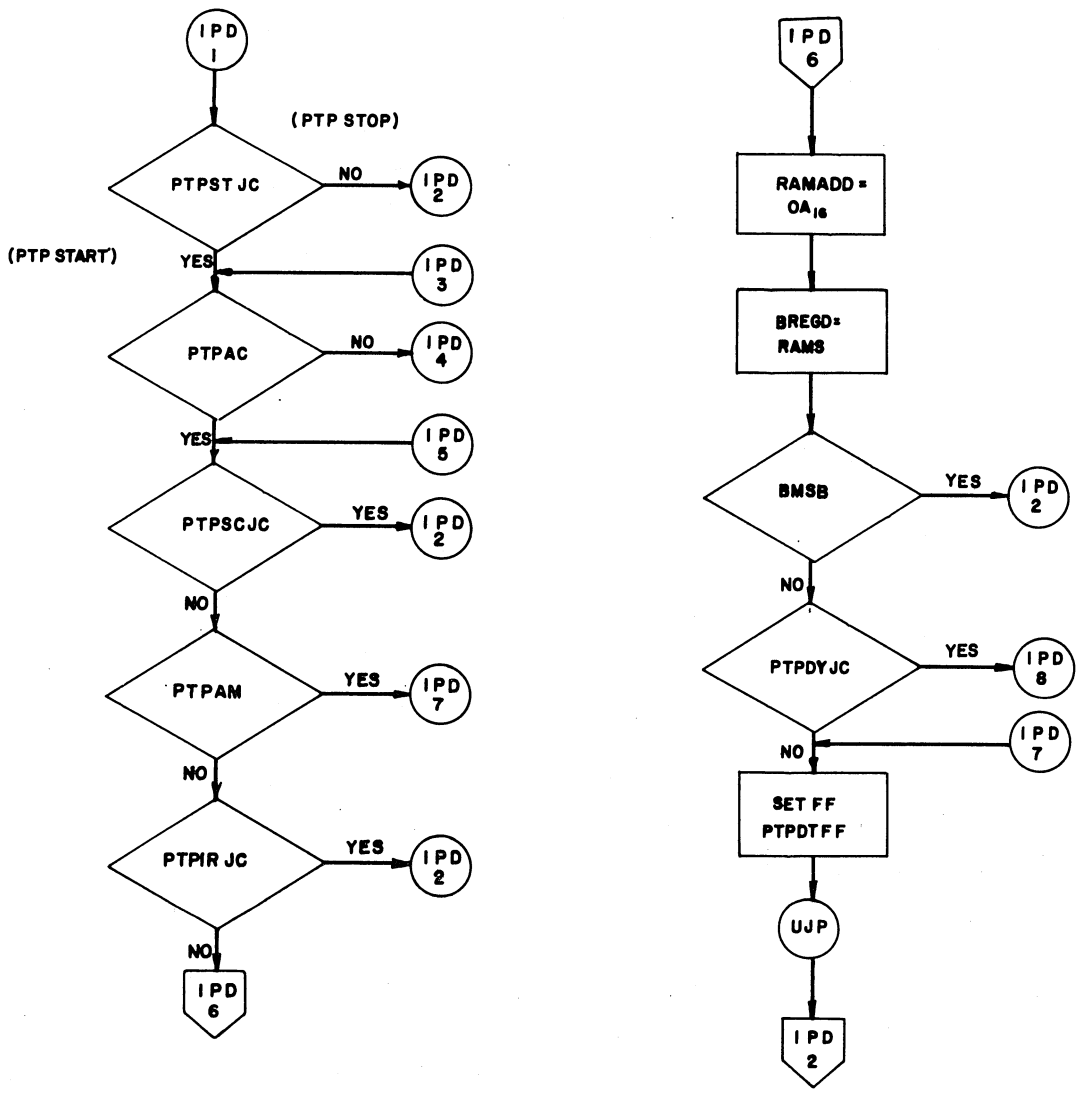


PTR INTERRUPT INTERNAL

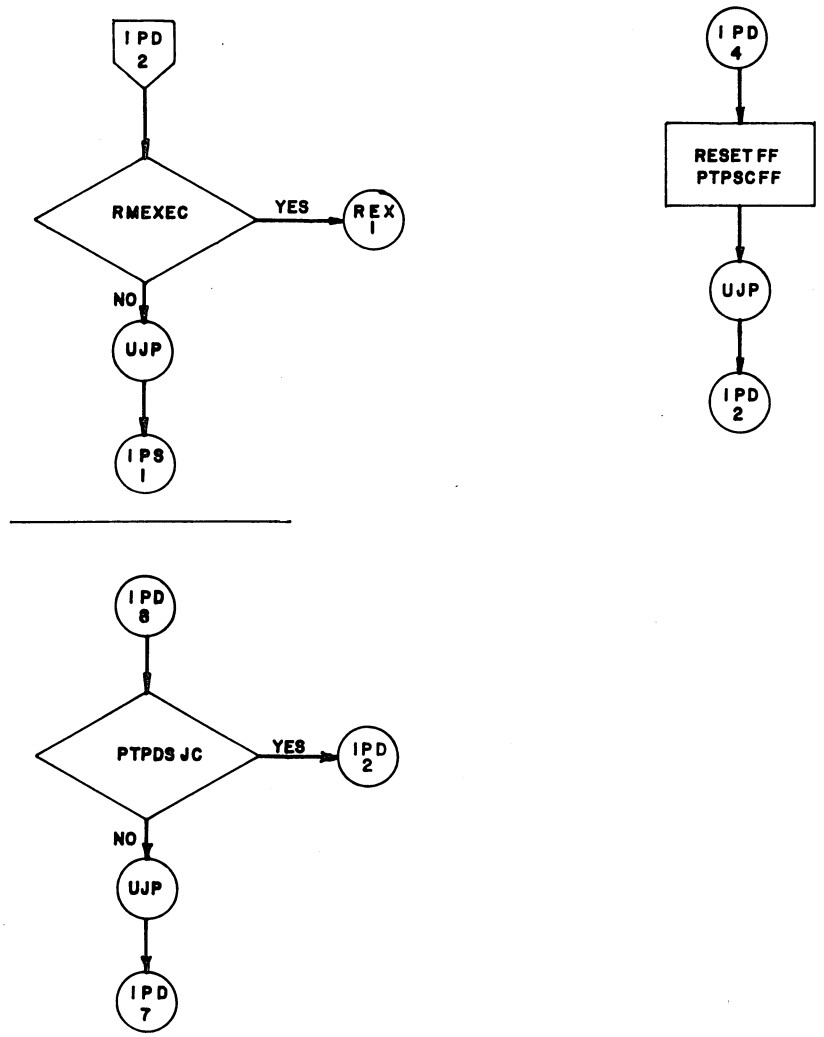




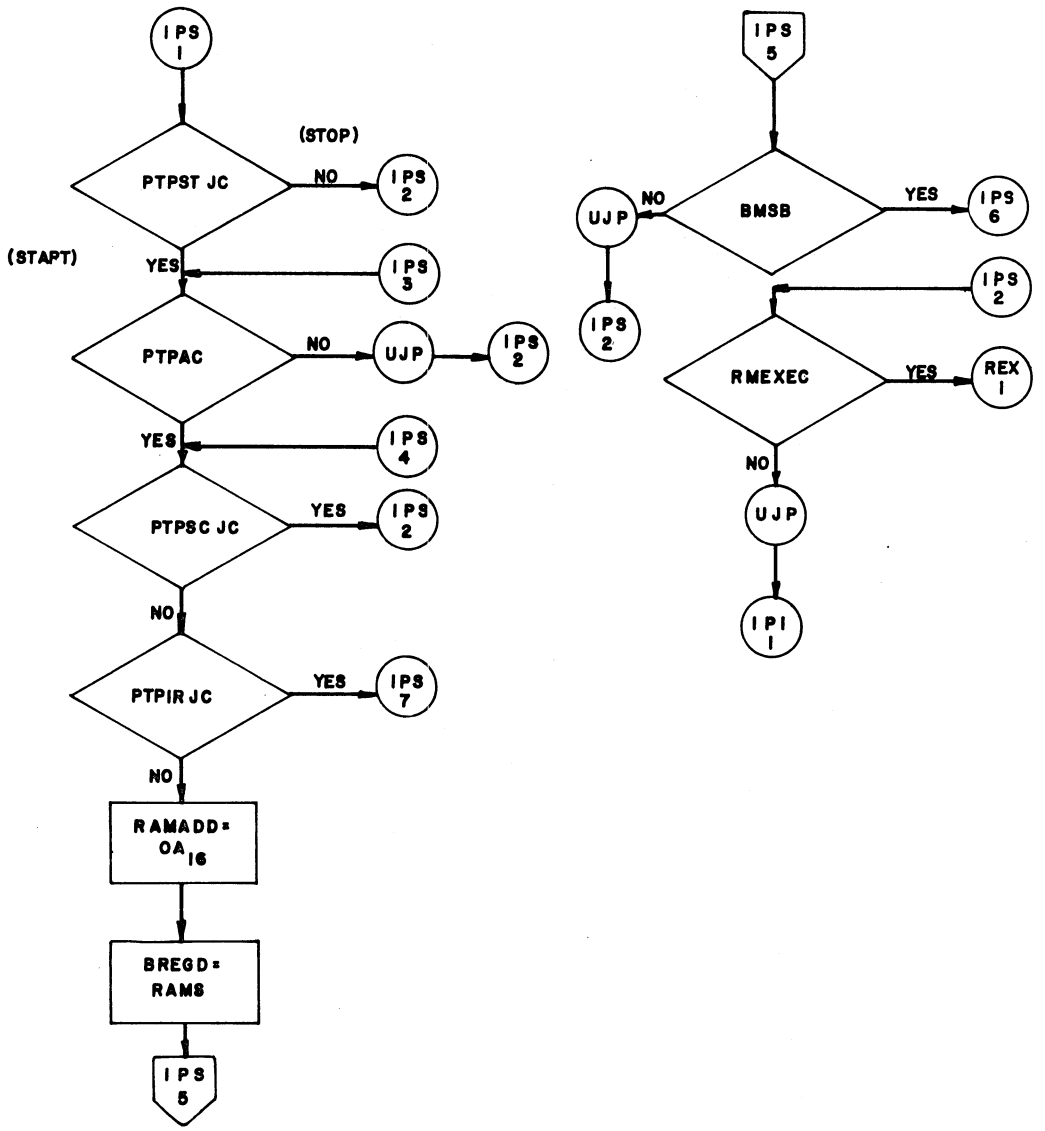
PTR INTERRUPT (CONTINUED)



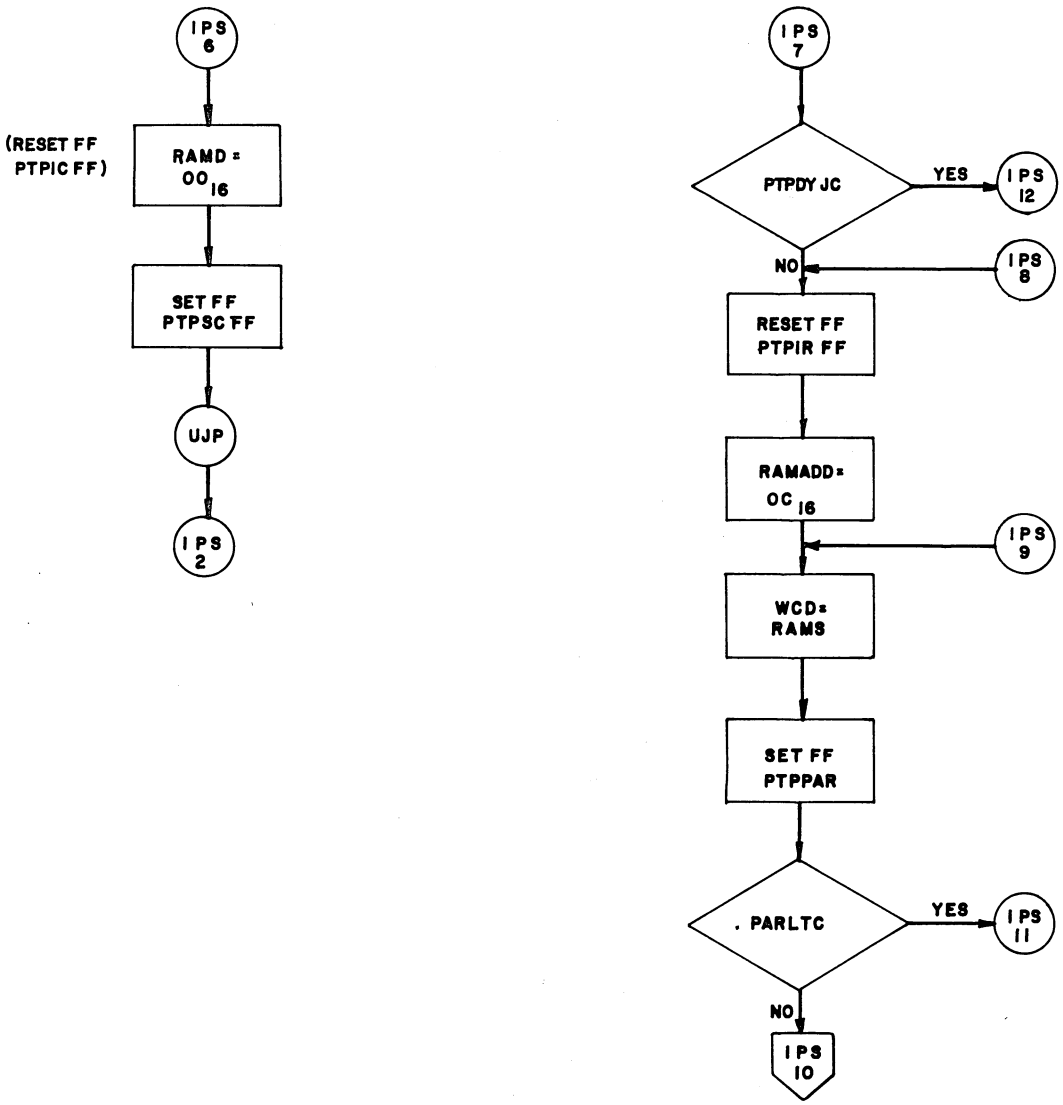
SET PTP DATA/FUNCTION STATUS INTERNAL



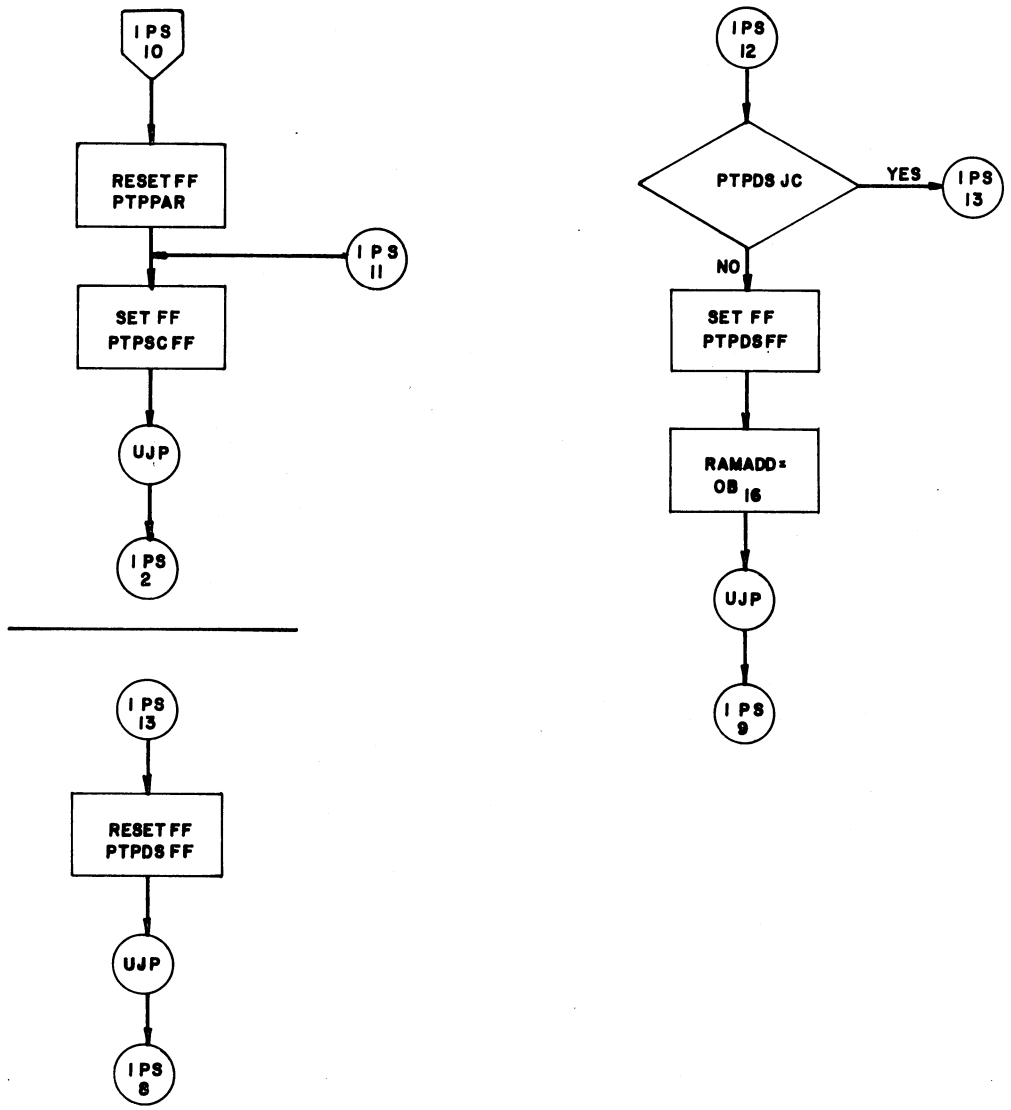
SET PTP DATA STATUS (CONTINUED)



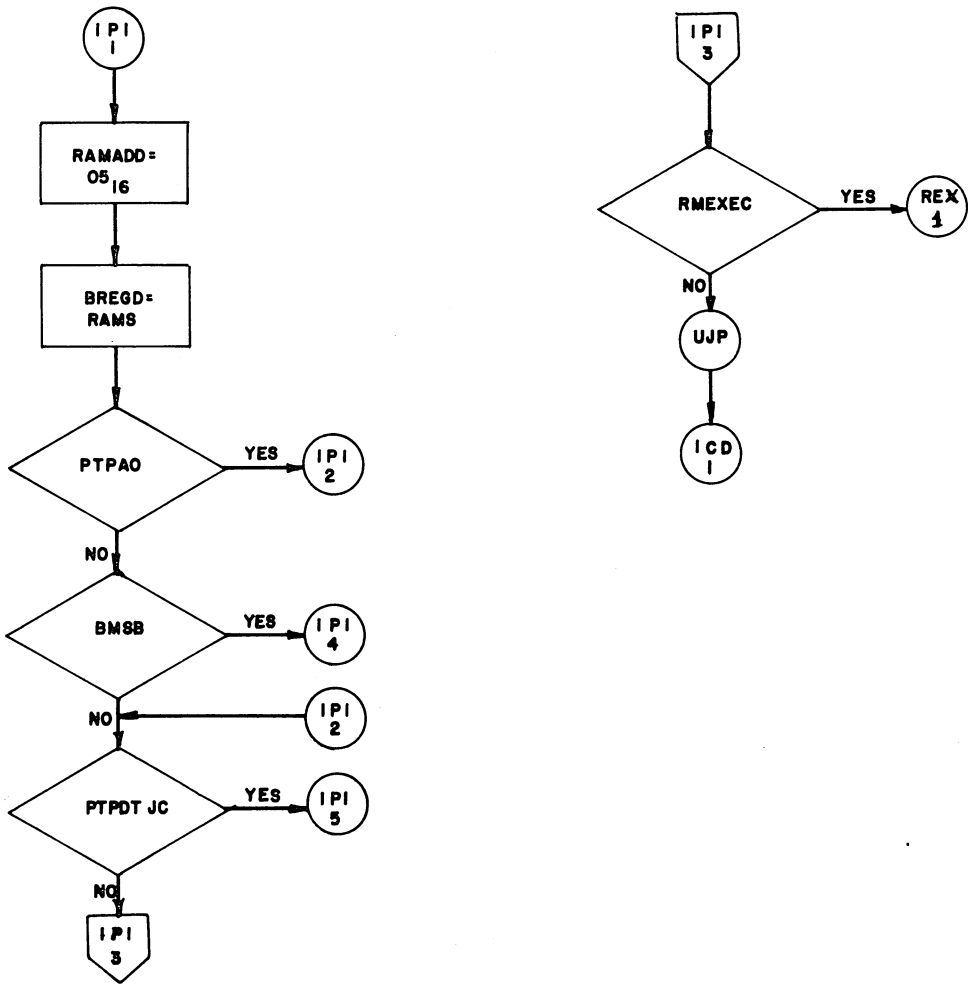
SET PTP SC INTERNAL



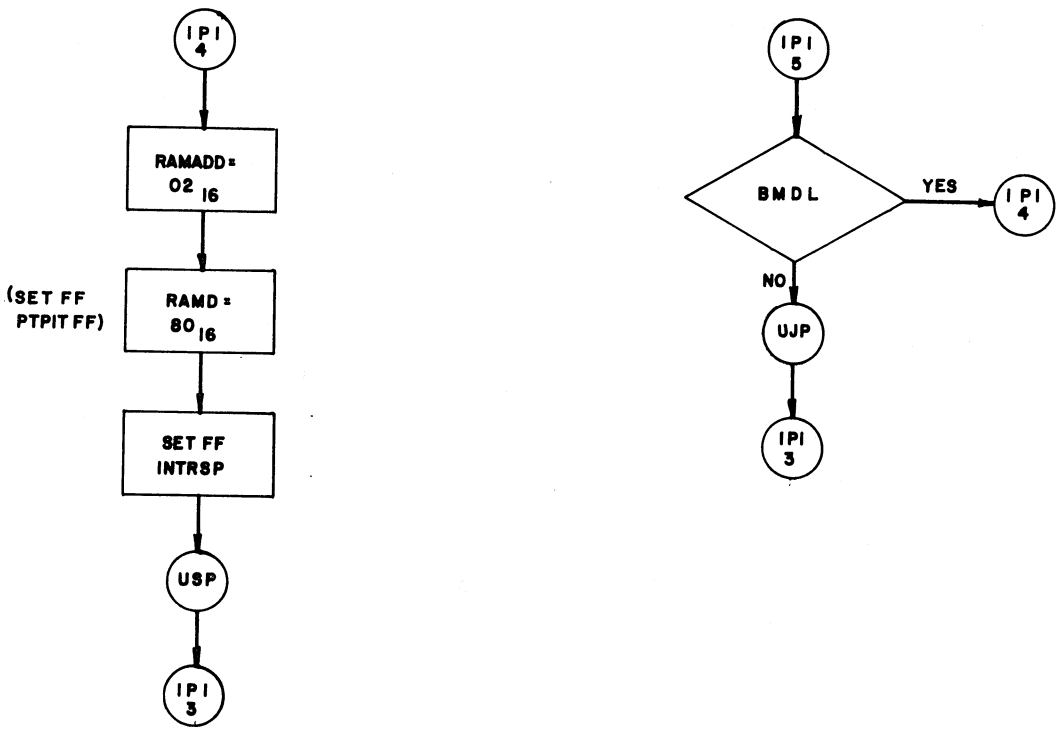
SET PTP SC (CONTINUED)



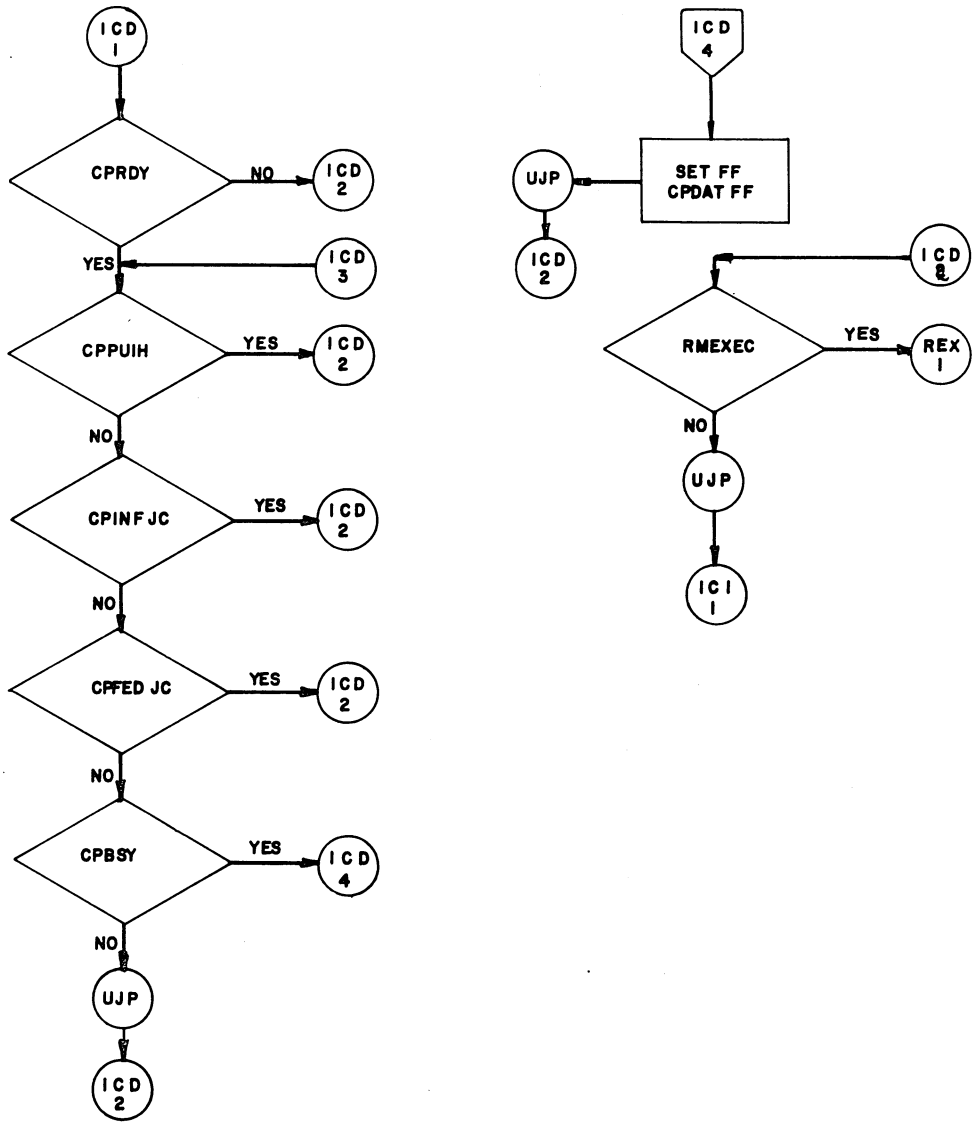
SET PTP SC (CONTINUED)



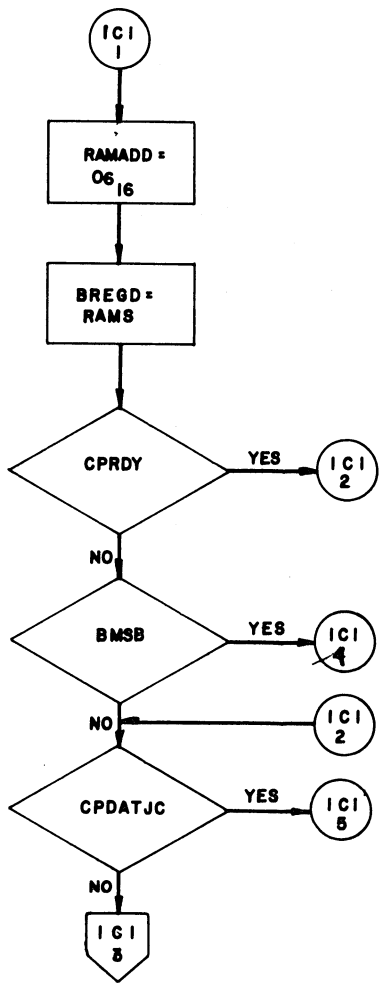
PTP INTERRUPT INTERNAL

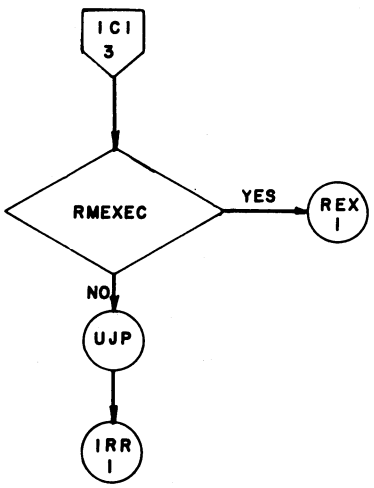


PTP INTERRUPT (CONTINUED)

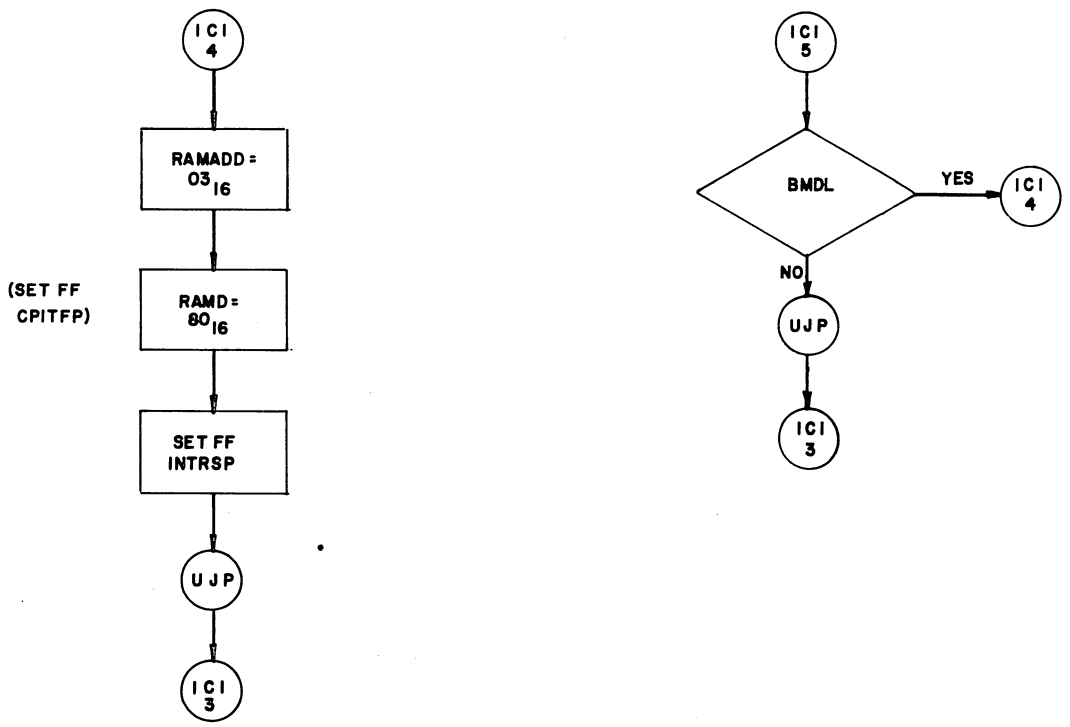


SET CP DATA STATUS, INTERNAL

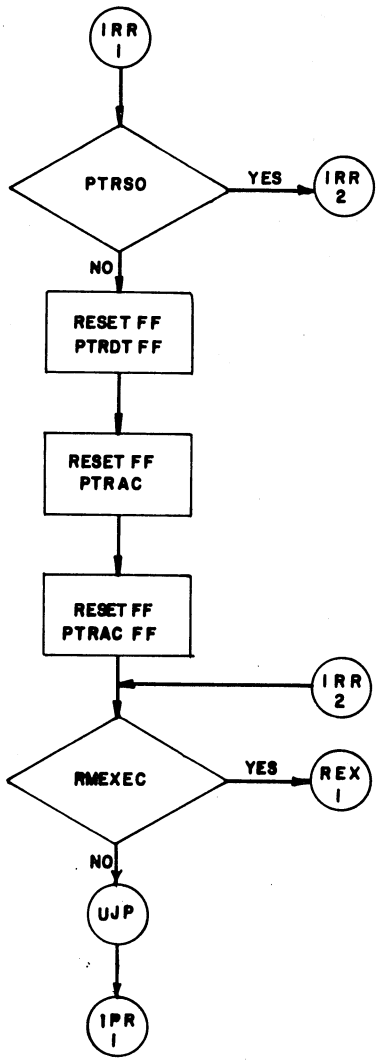




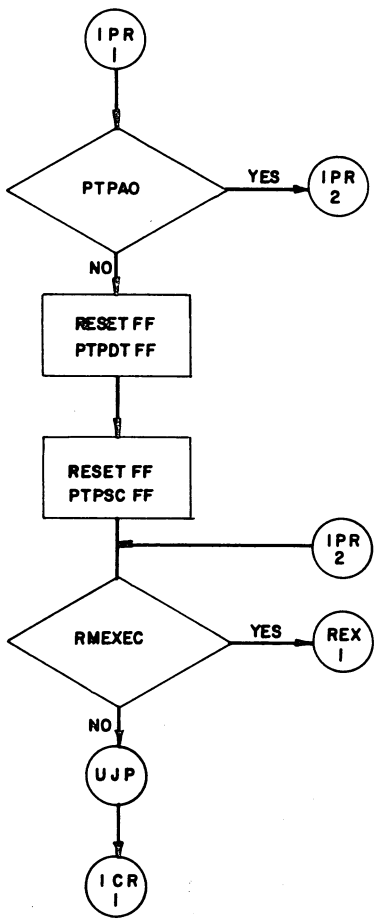
CP INTERRUPT, INTERNAL



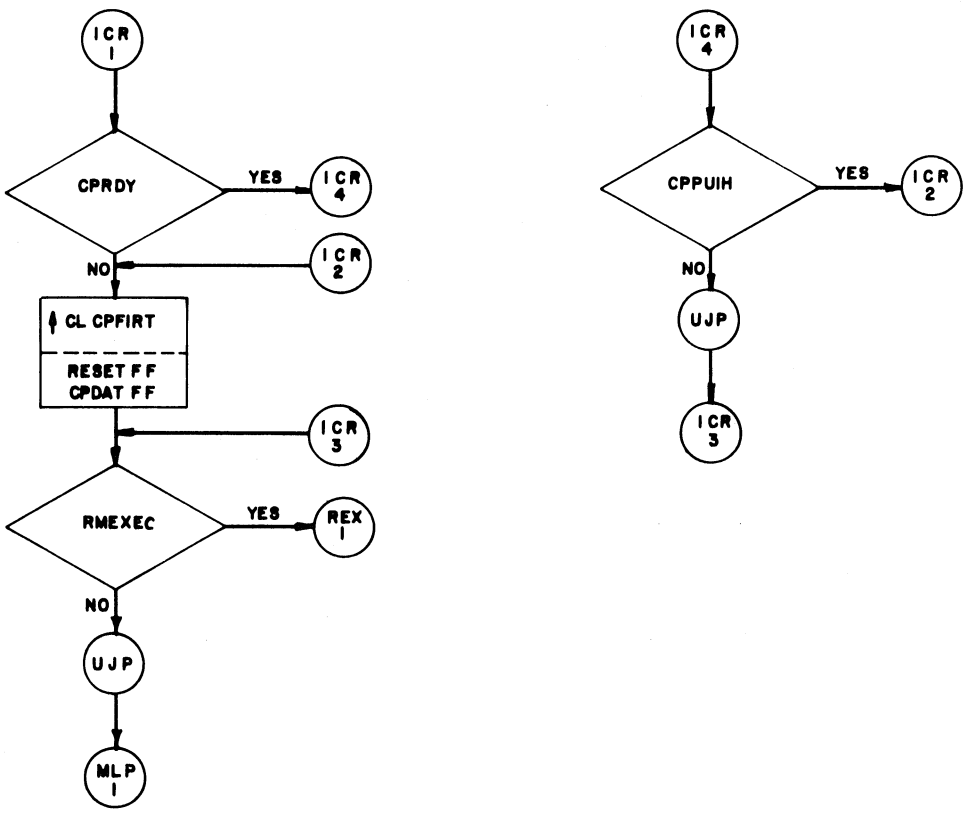
CP INTERRUPT (CONTINUED)



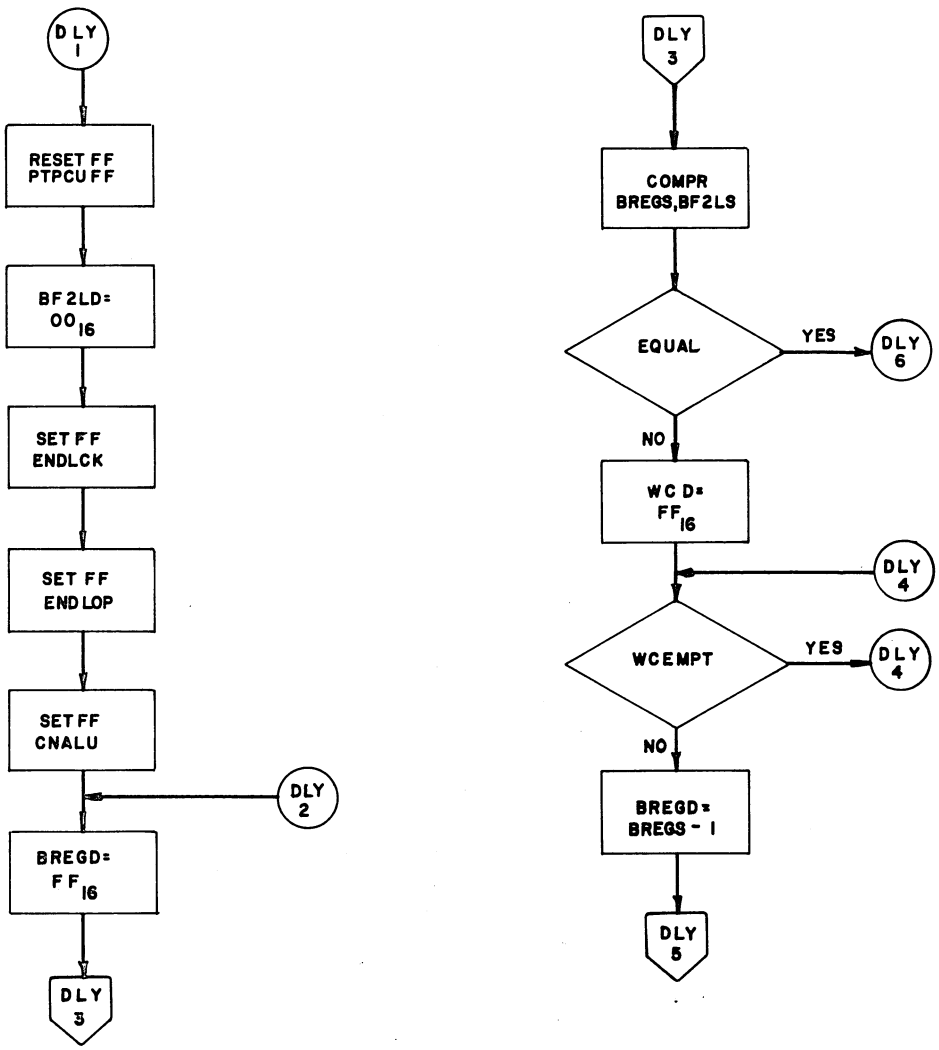
PTR READY STATUS, INTERNAL



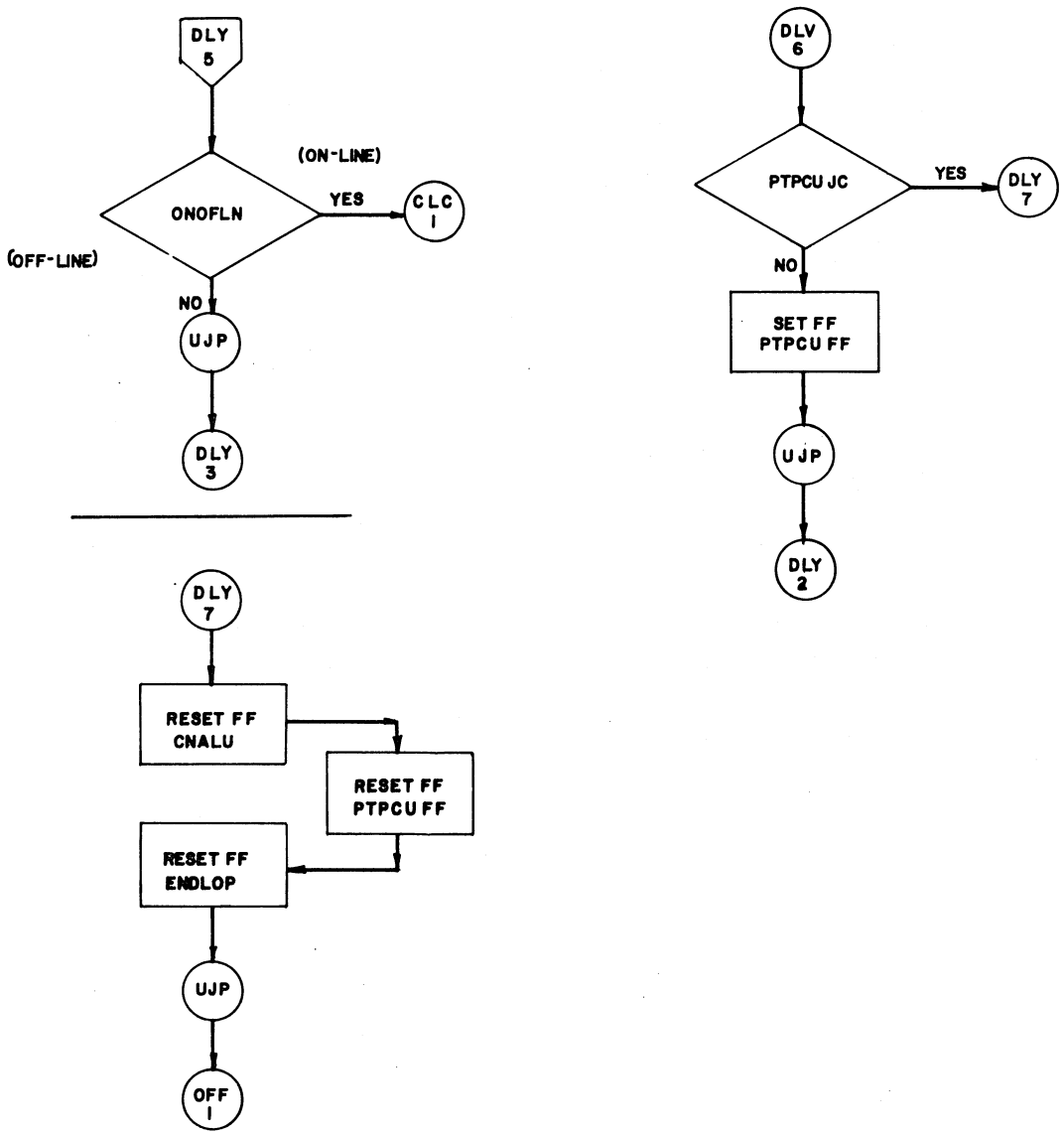
PTP READY STATUS, INTERNAL



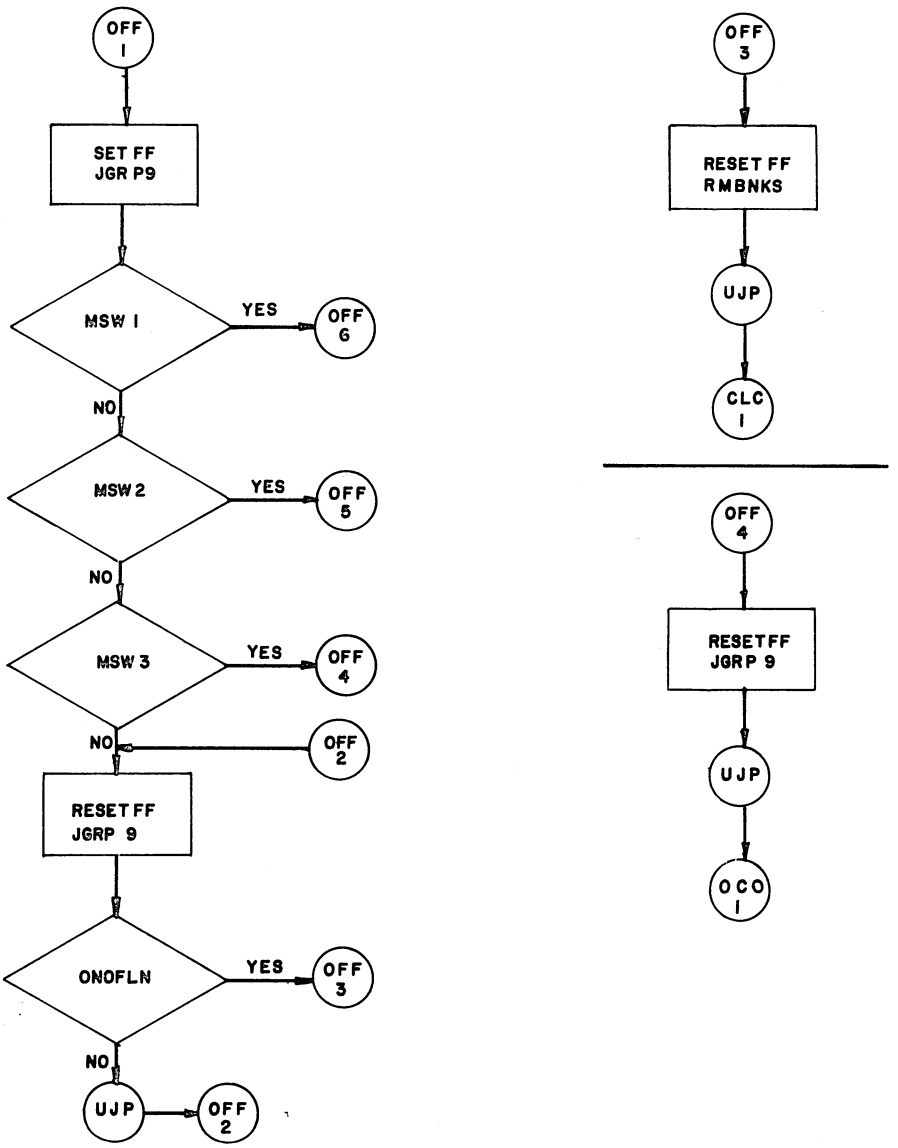
CP READY STATUS, INTERNAL



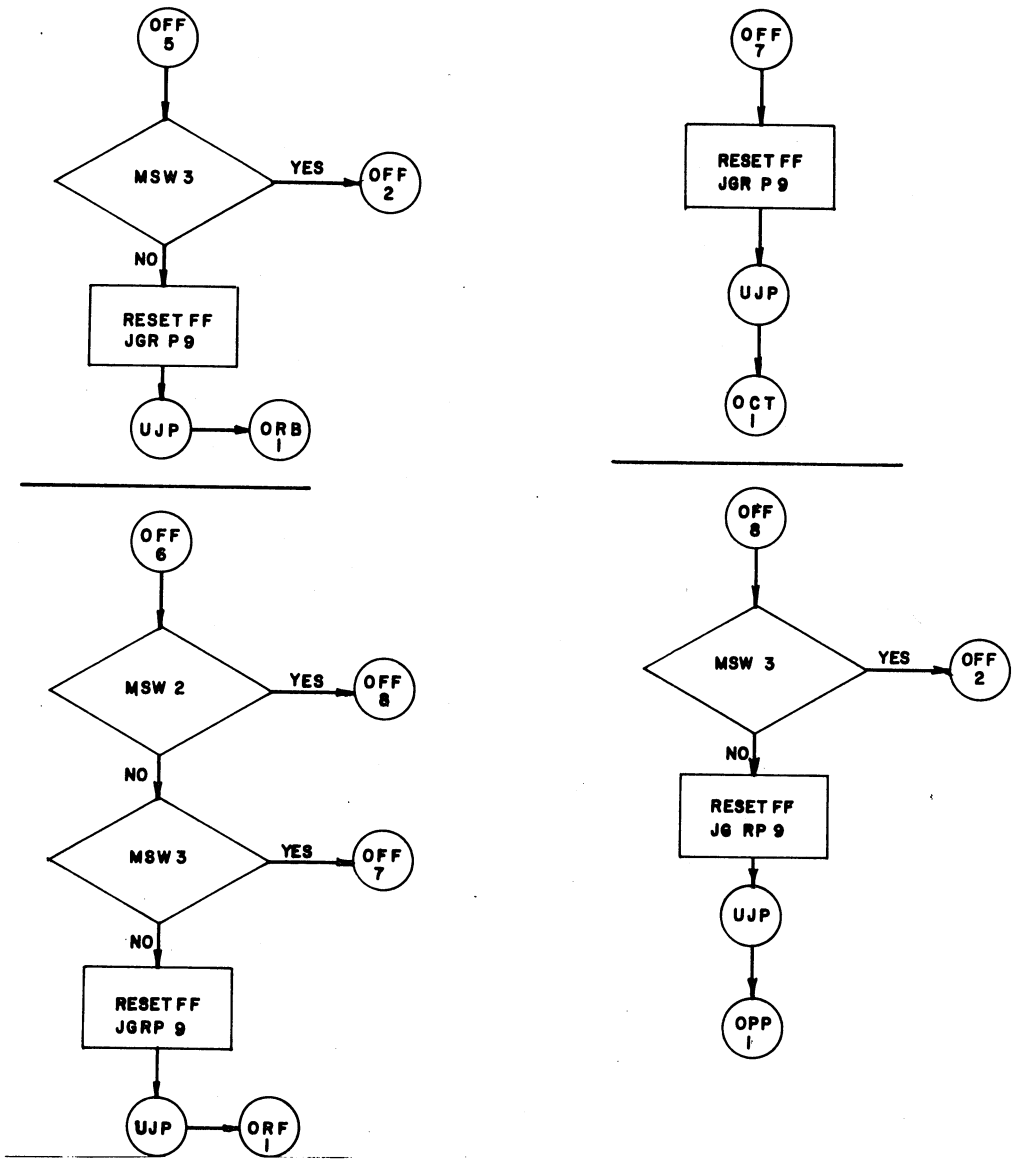
DELAY INTERNAL



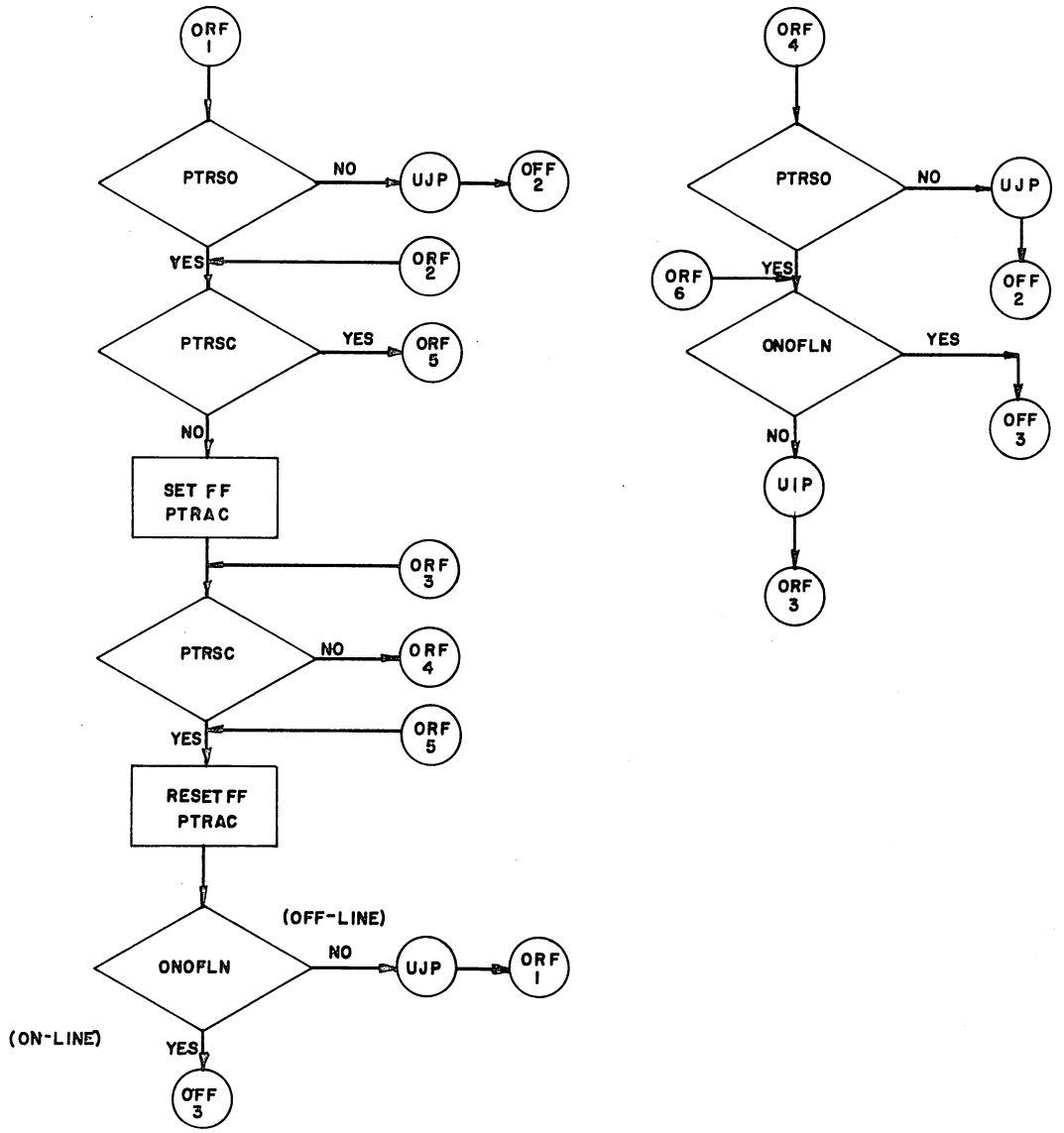
DELAY INTERRUPT (CONTINUED)



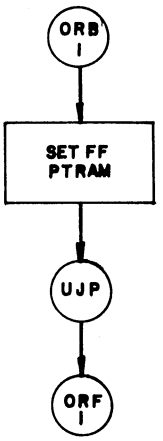
SELECT OFF-LINE MAINTENANCE ROUTINE INTERNAL



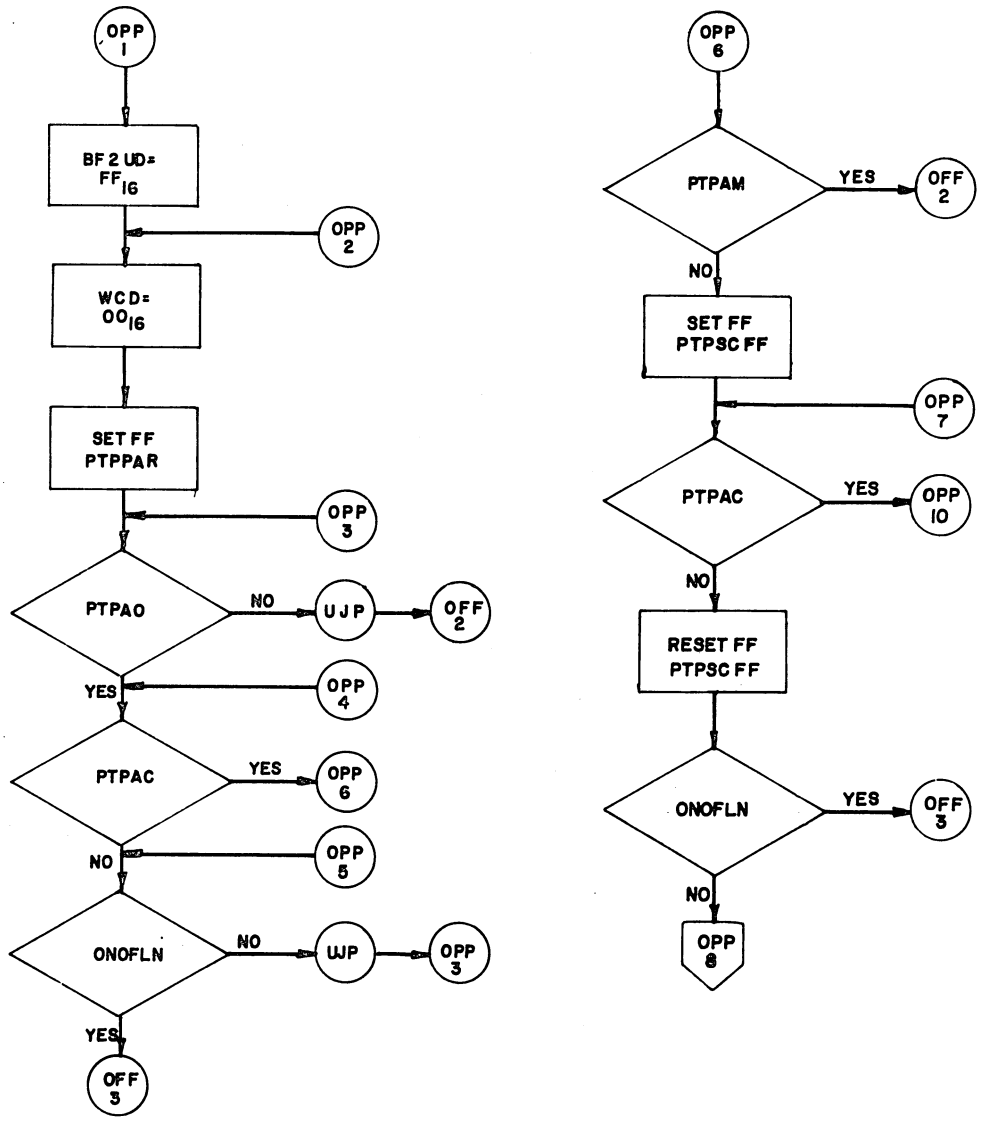
SELECT OFF-LINE MAINTENANCE ROUTINE INTERNAL (CONTINUED)



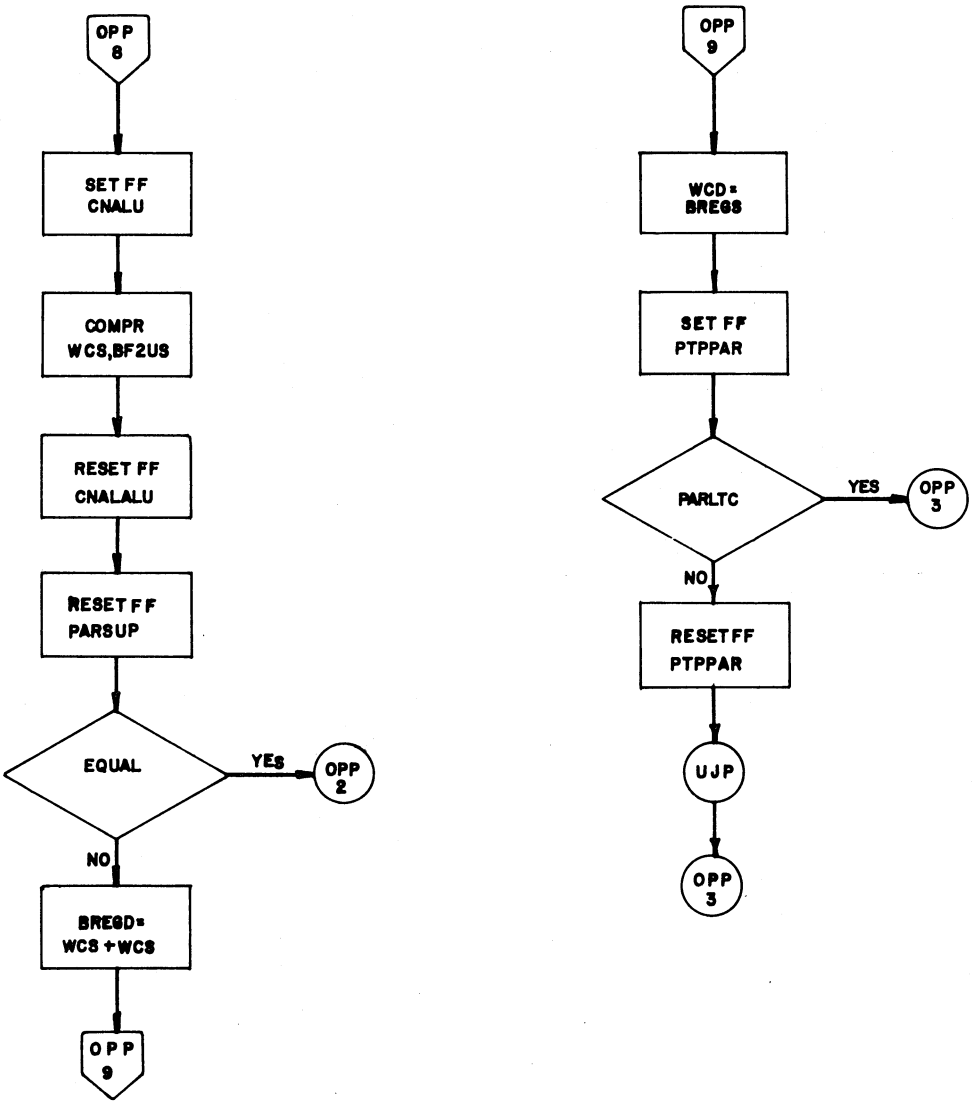
OFF LINE PTR FORWARD MOTION



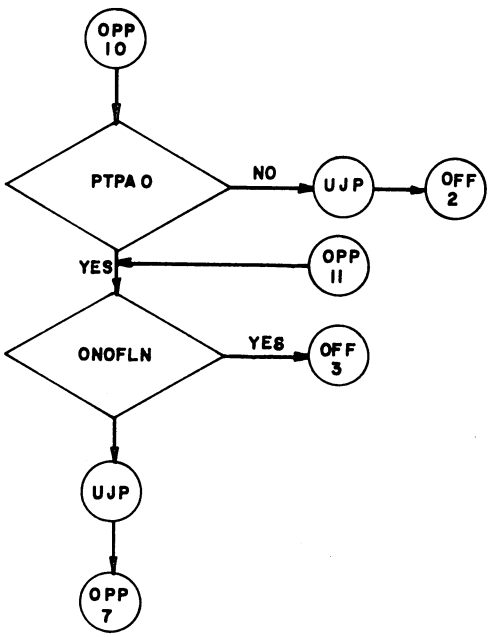
OFF LINE BACKWARD MOTION



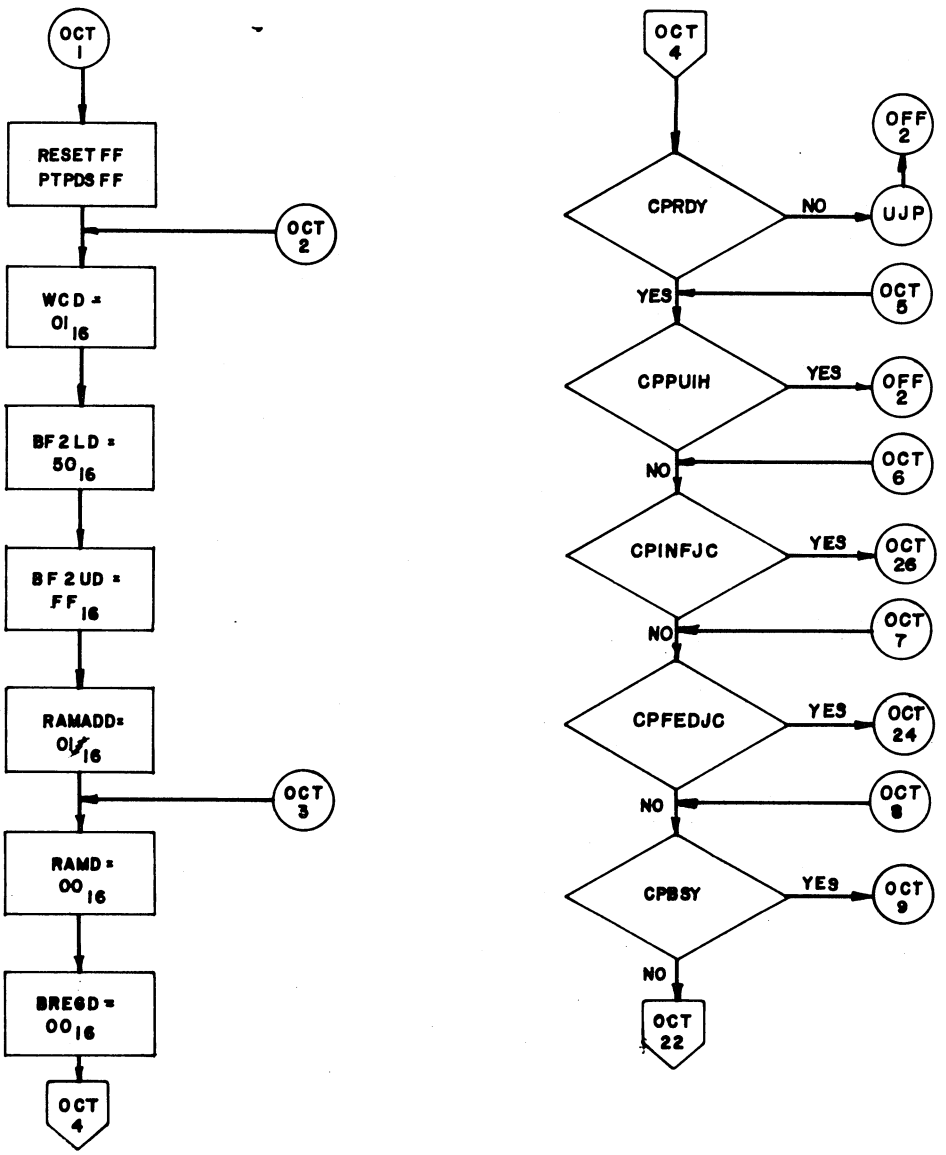
OFF LINE PTP TRIANGLE PUNCHING


OPP 8
SET FF CNALU
COMPR WCS,BF2US
RESET FF CNALALU
RESET FF PARSUP
EQUAL
YES
OPP 2
NO
BREGD= WCS+WCS
OPP 9
OPP 9
WCD= BREGS
SET FF PTPPAR
PARLTC
YES
OPP 3
NO
RESET FF PTPPAR
UJP
OPP 3

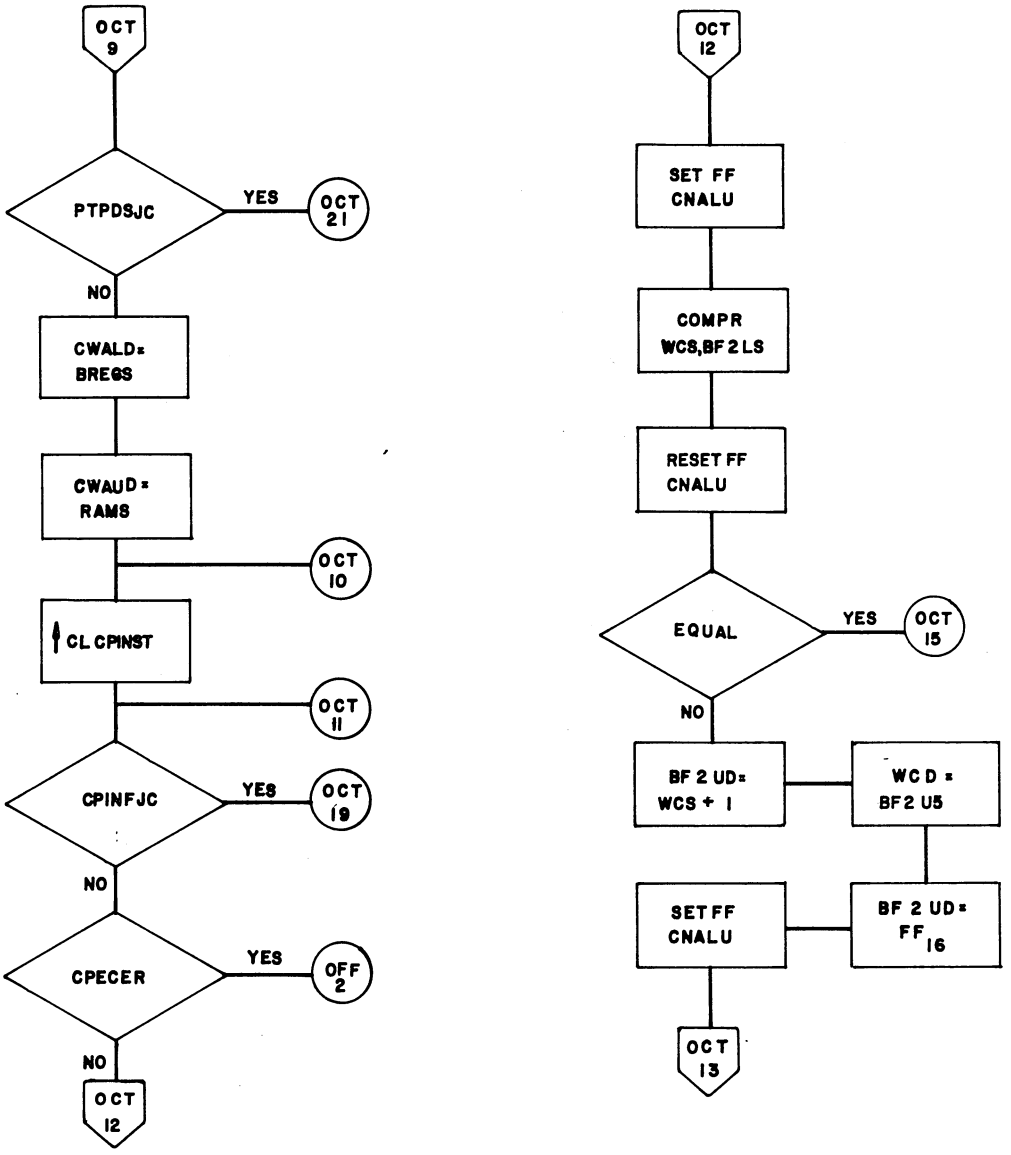
OFF LINE PTP



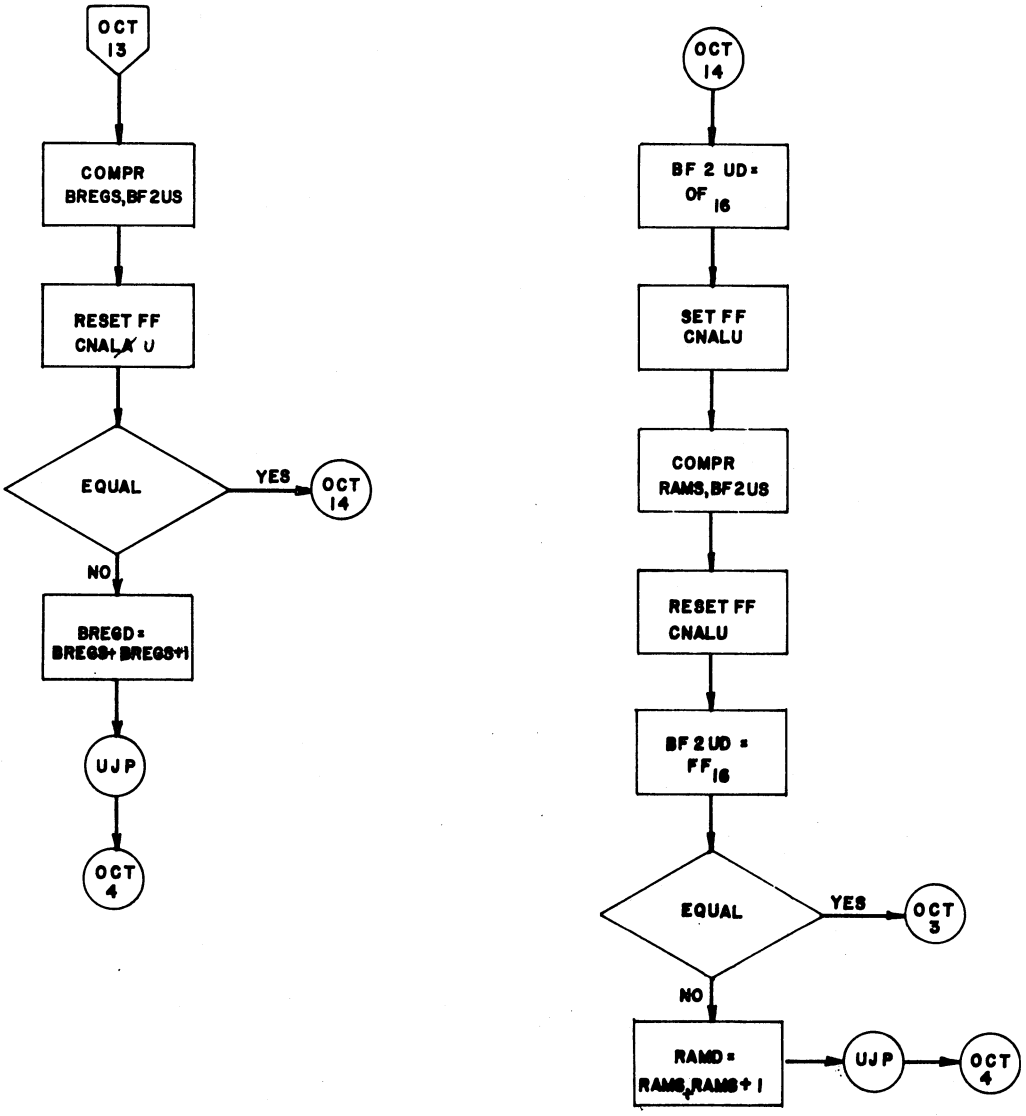
OFF LINE PTP



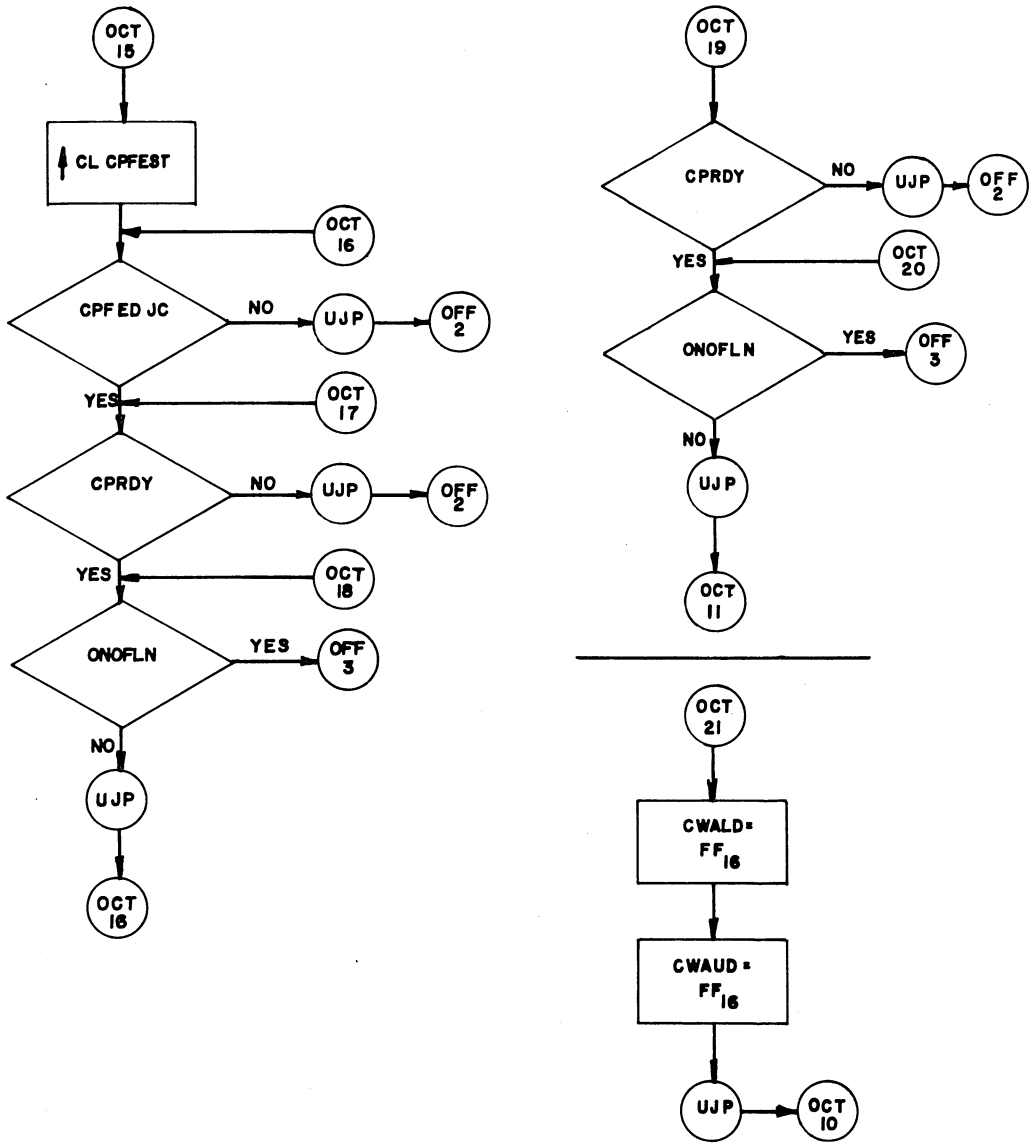
OFF LINE CP TRIANGLE PUNCHING



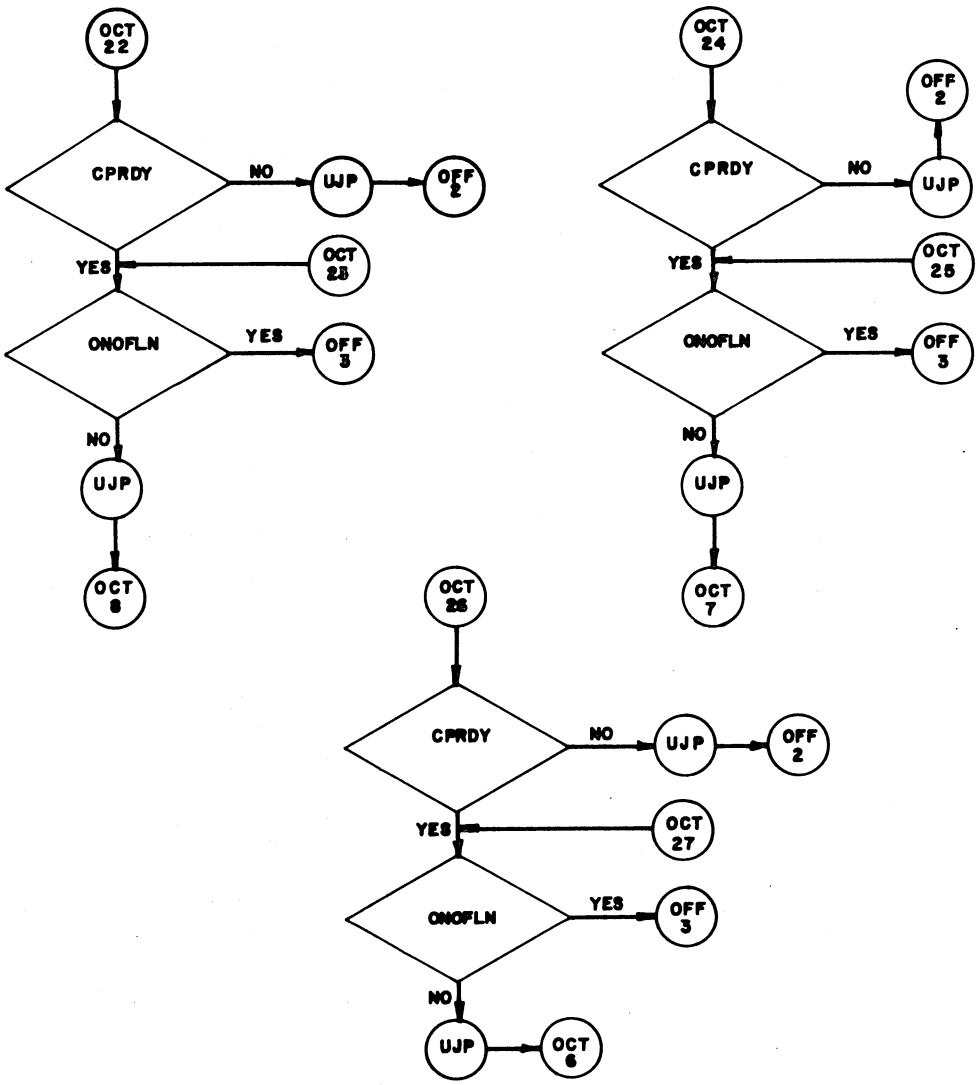
OFF LINE CP TRIANGLE (CONTINUED)



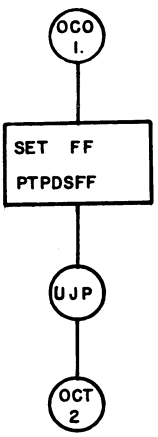
OFF LINE CP TRIANGLE (CONTINUED)



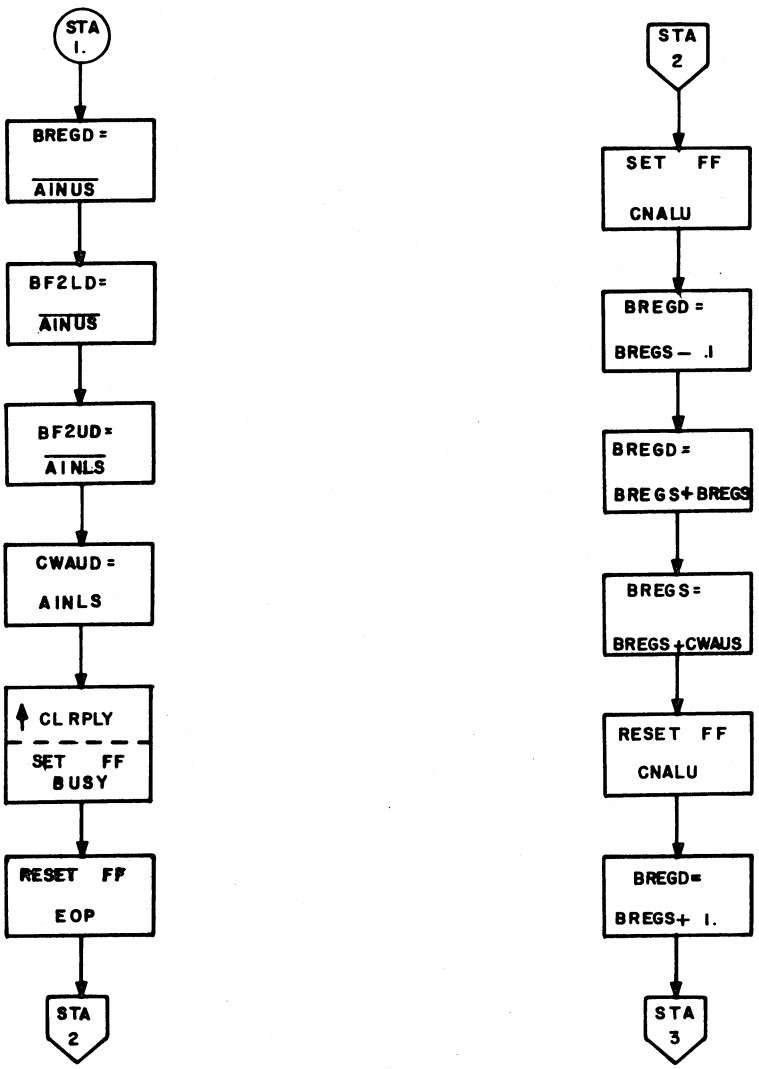
OFF LINE CP TRIANGLE (CONTINUED)



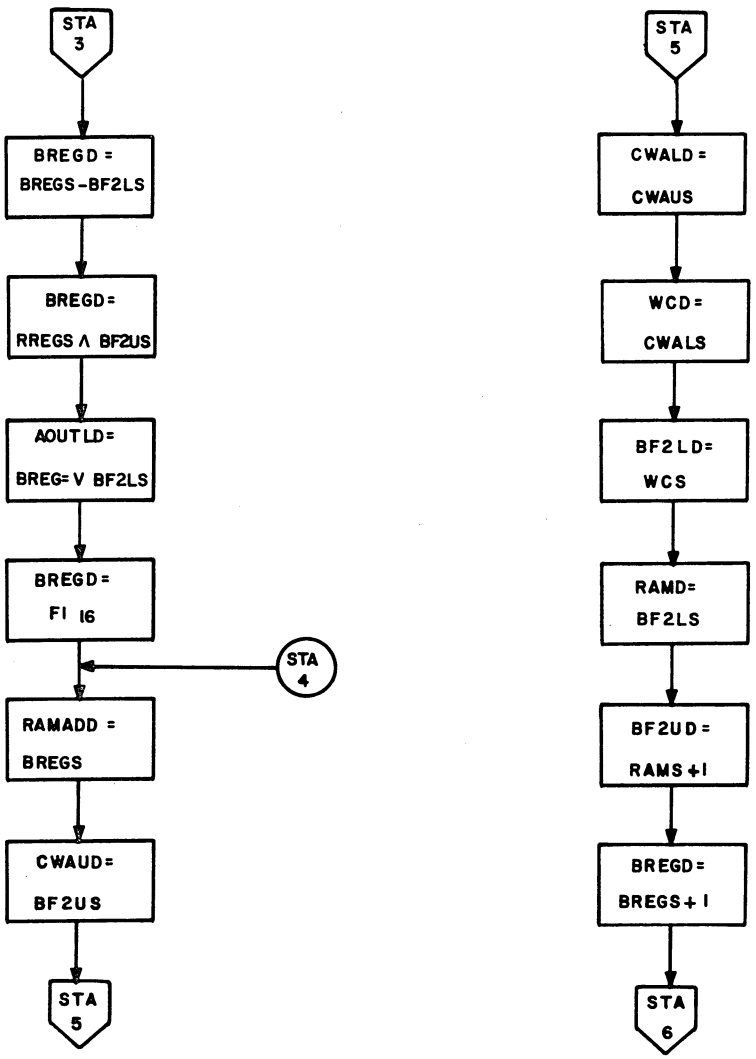
OFF LINE CP TRIANGLE (CONTINUED)



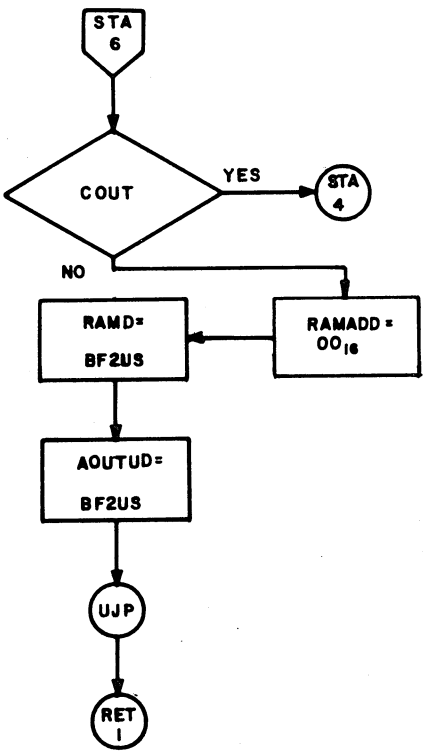
OFF LINE CP ALL ONES



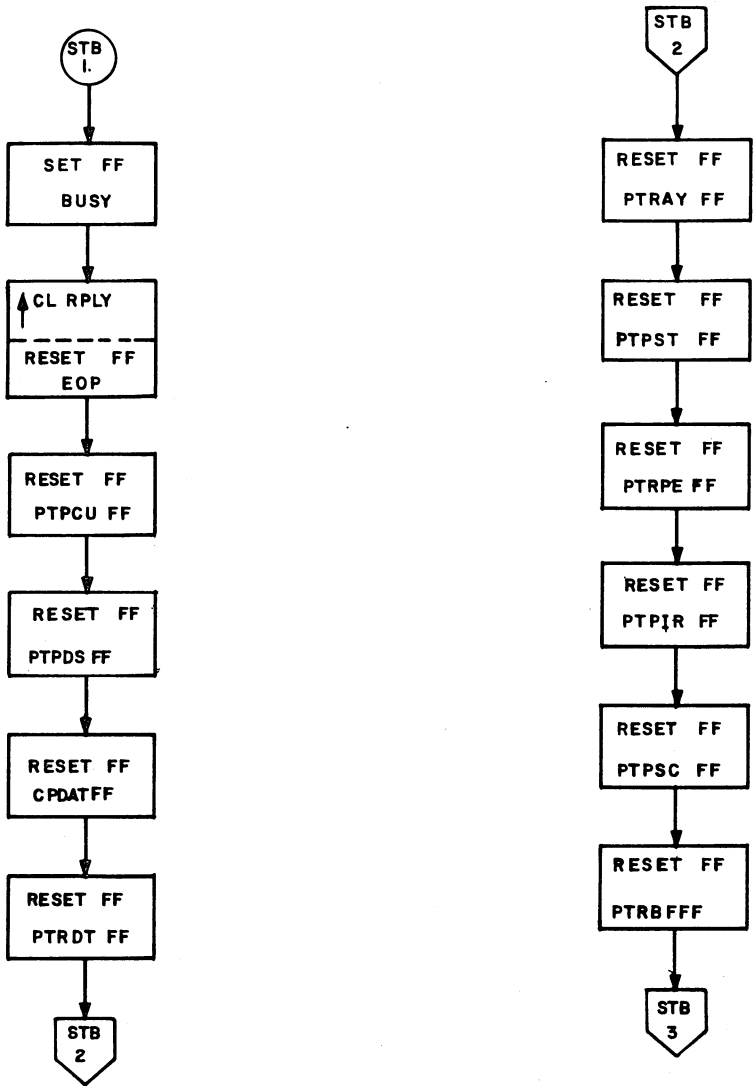
SELF TEST 1 A/Q COMMAND



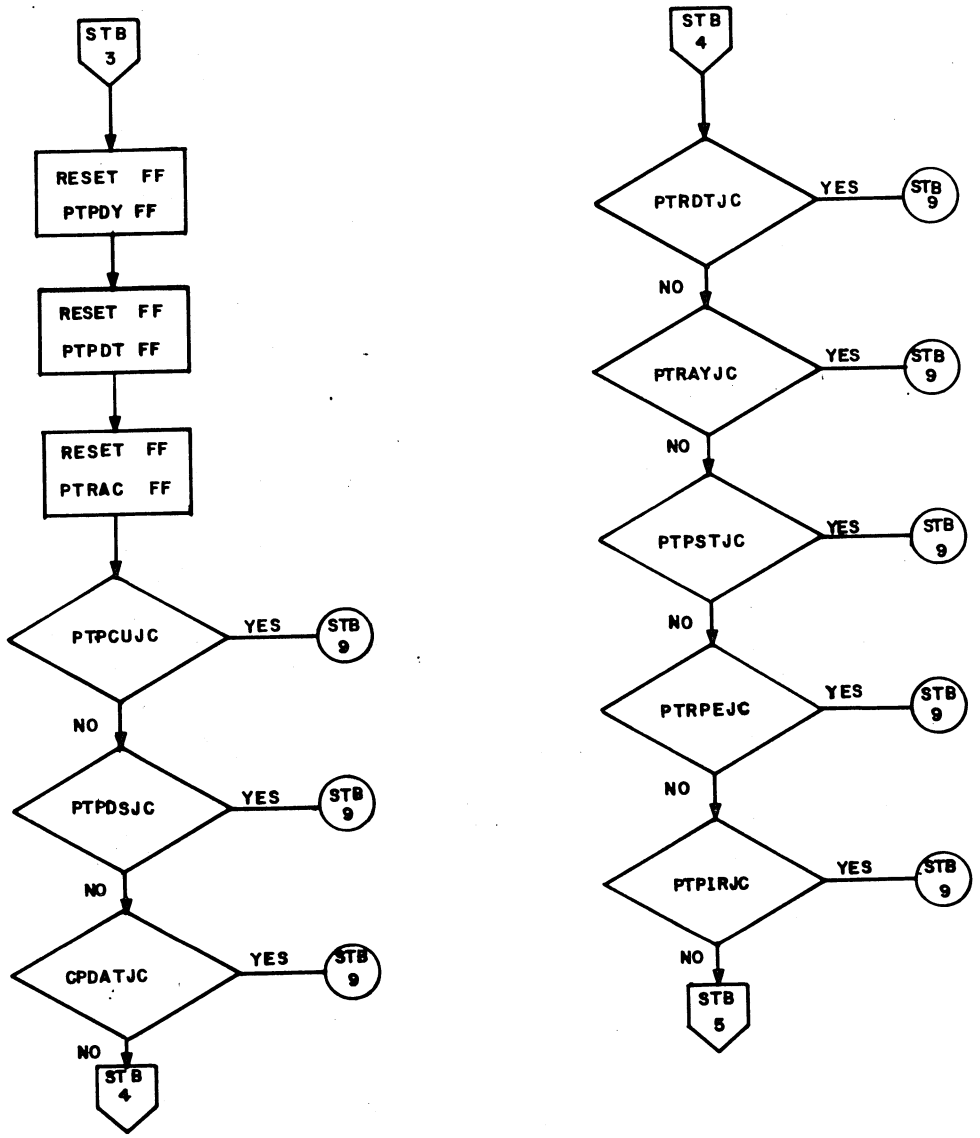
SELF TEST 1 A/Q COMMAND (CONTINUED)



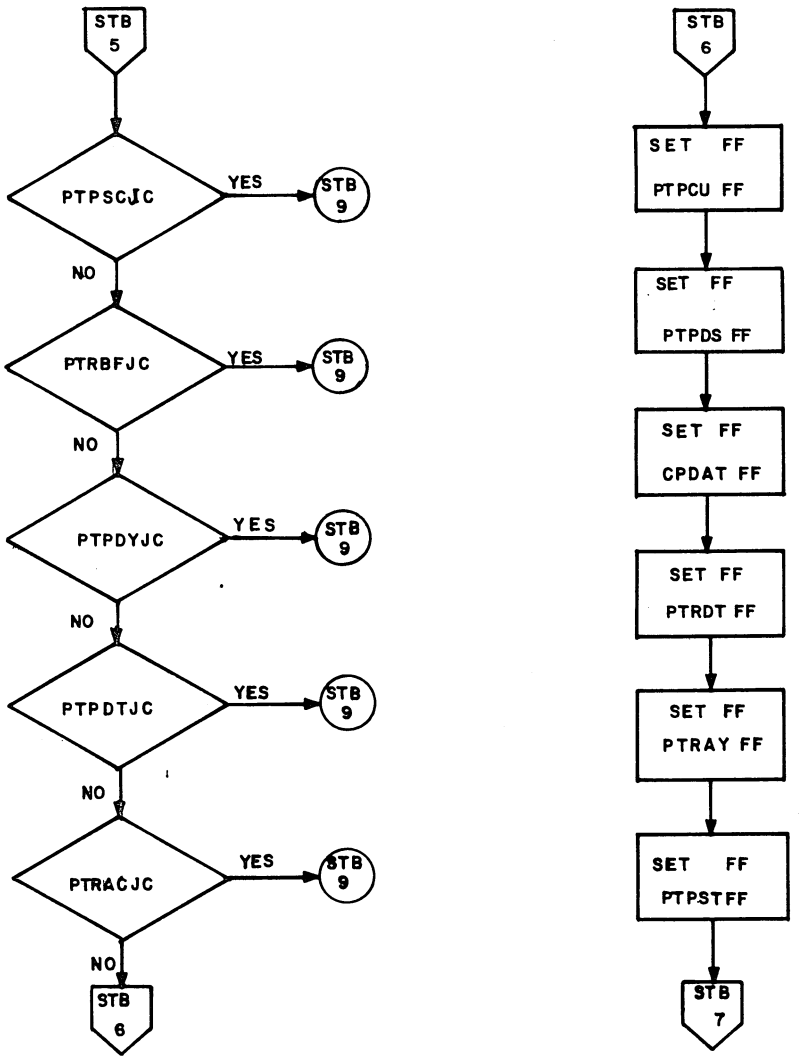
SELF TEST 1 A/Q COMMAND (CONTINUED)


STB 1.
SET FF BUSY
CL RPLY
RESET FF EOP
RESET FF PTPCU FF
RESET FF PTPDS FF
RESET FF CPDATFF
RESET FF PTRDT FF
STB 2
STB 2
RESET FF PTRAY FF
RESET FF PTPST FF
RESET FF PTRPE FF
RESET FF PTPIR FF
RESET FF PTPSC FF
RESET FF PTRBFFF
STB 3

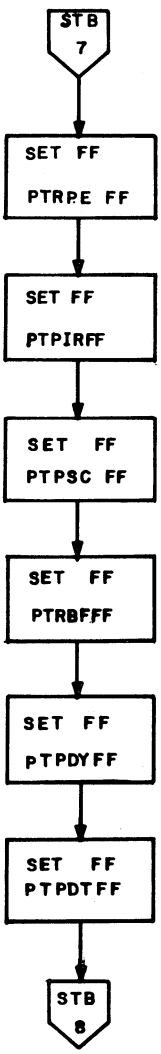
Self Test 2

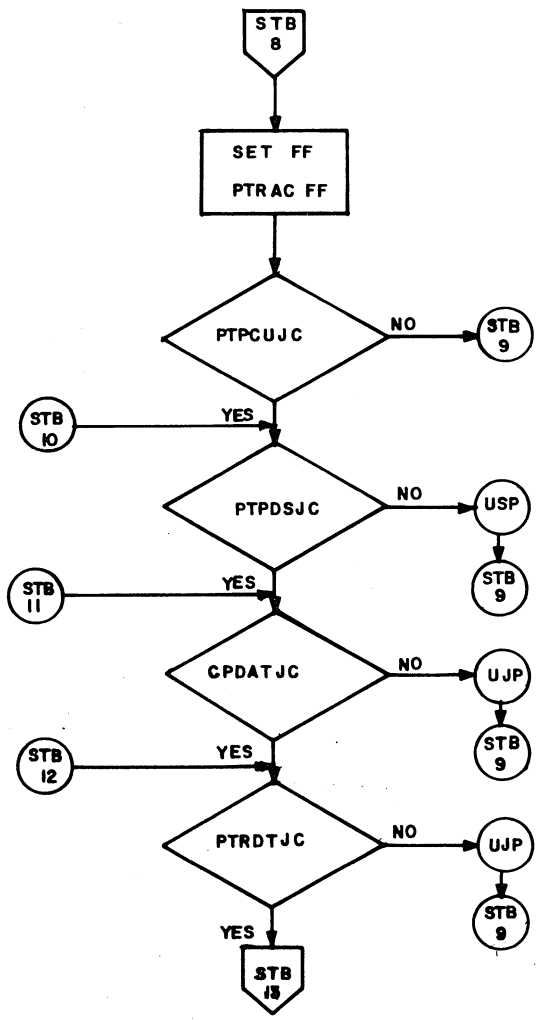


SELF TEST 2 (CONTINUED)

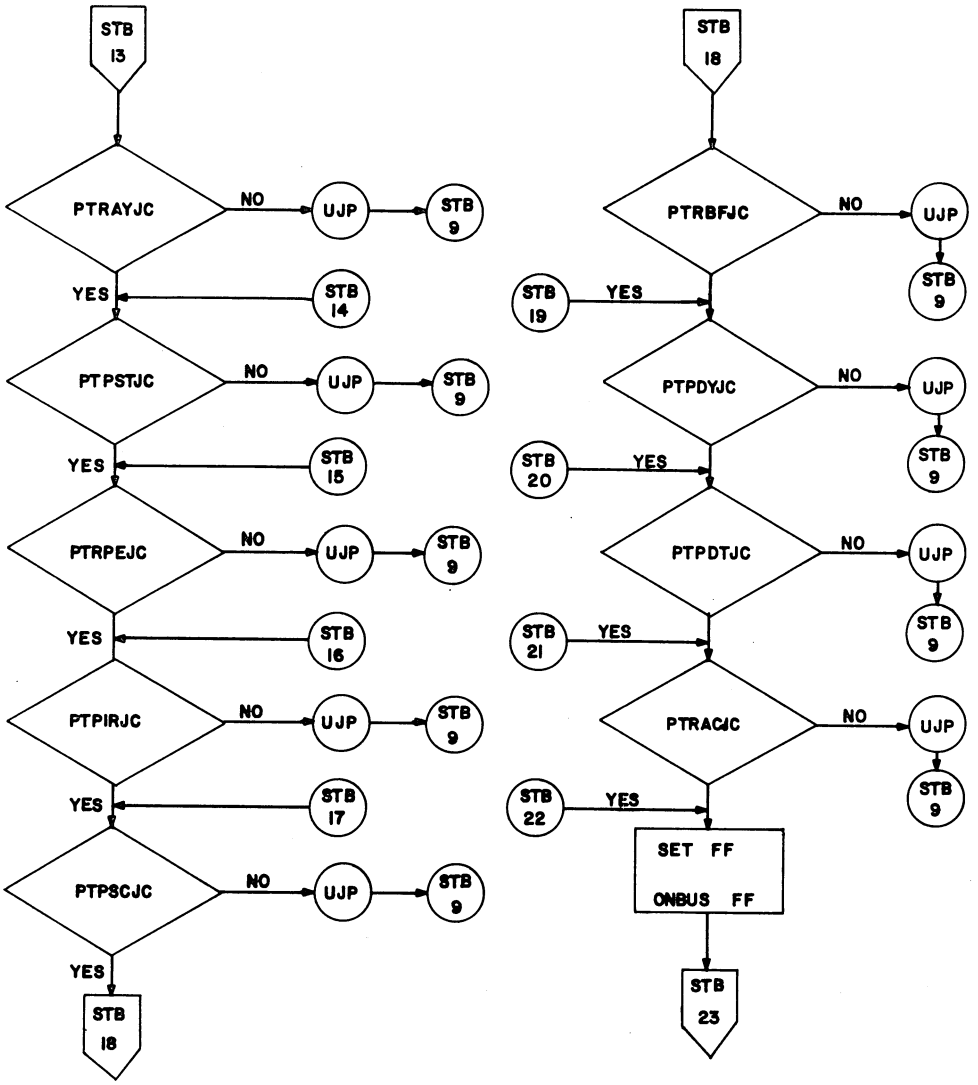


SELF TEST 2 (CONTINUED)

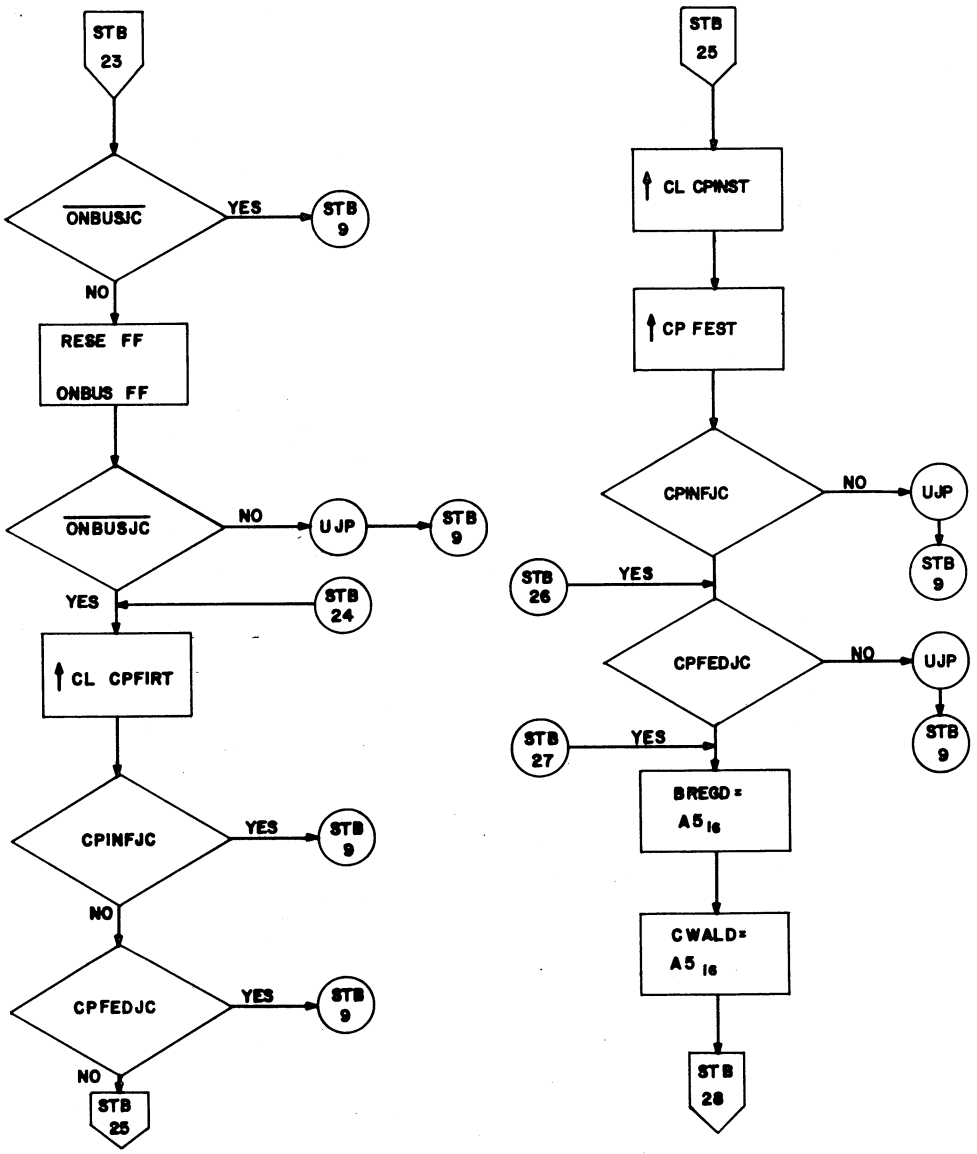




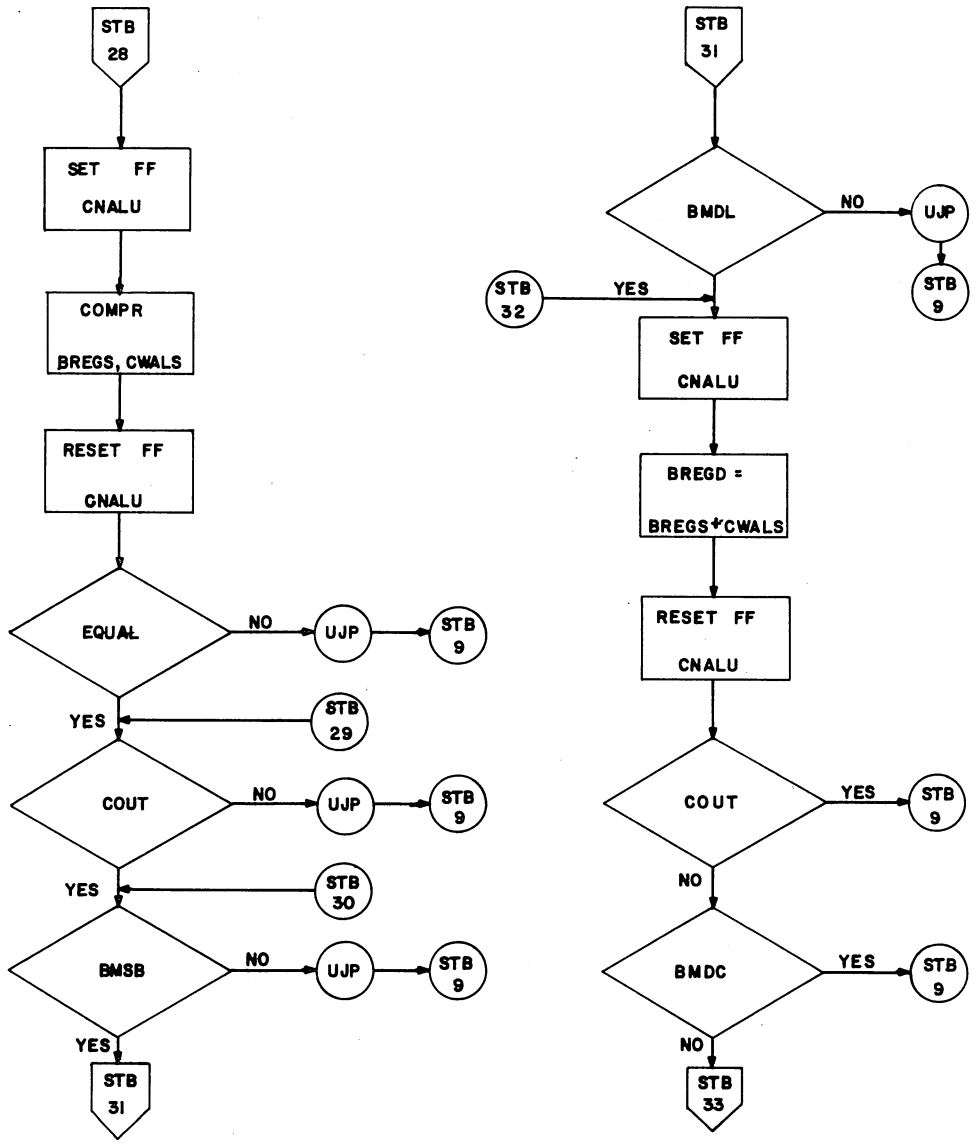
SELF TEST 2 (CONTINUED)



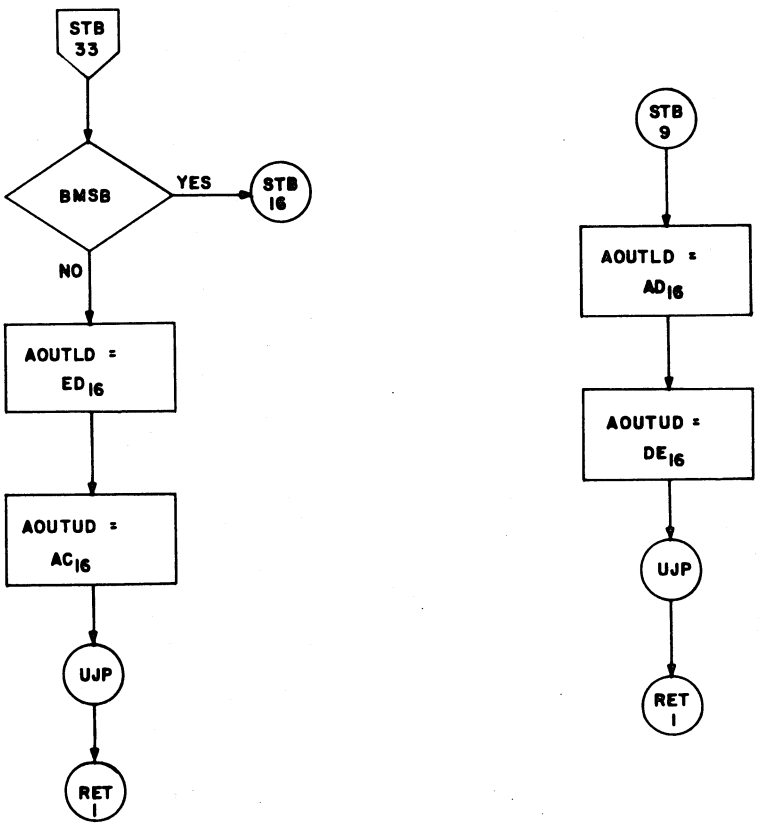
SELF TEST 2 (CONTINUED)



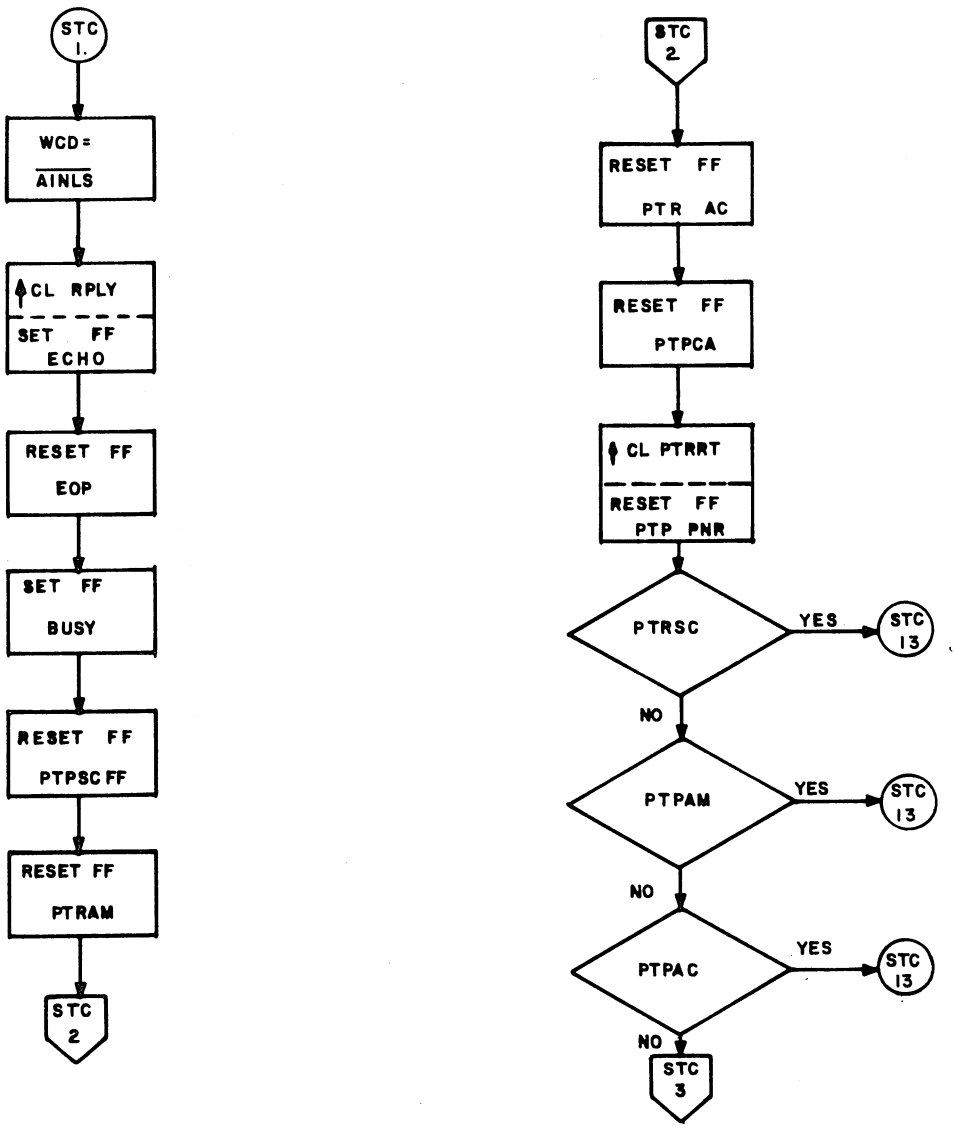
SELF TEST 2 (CONTINUED)



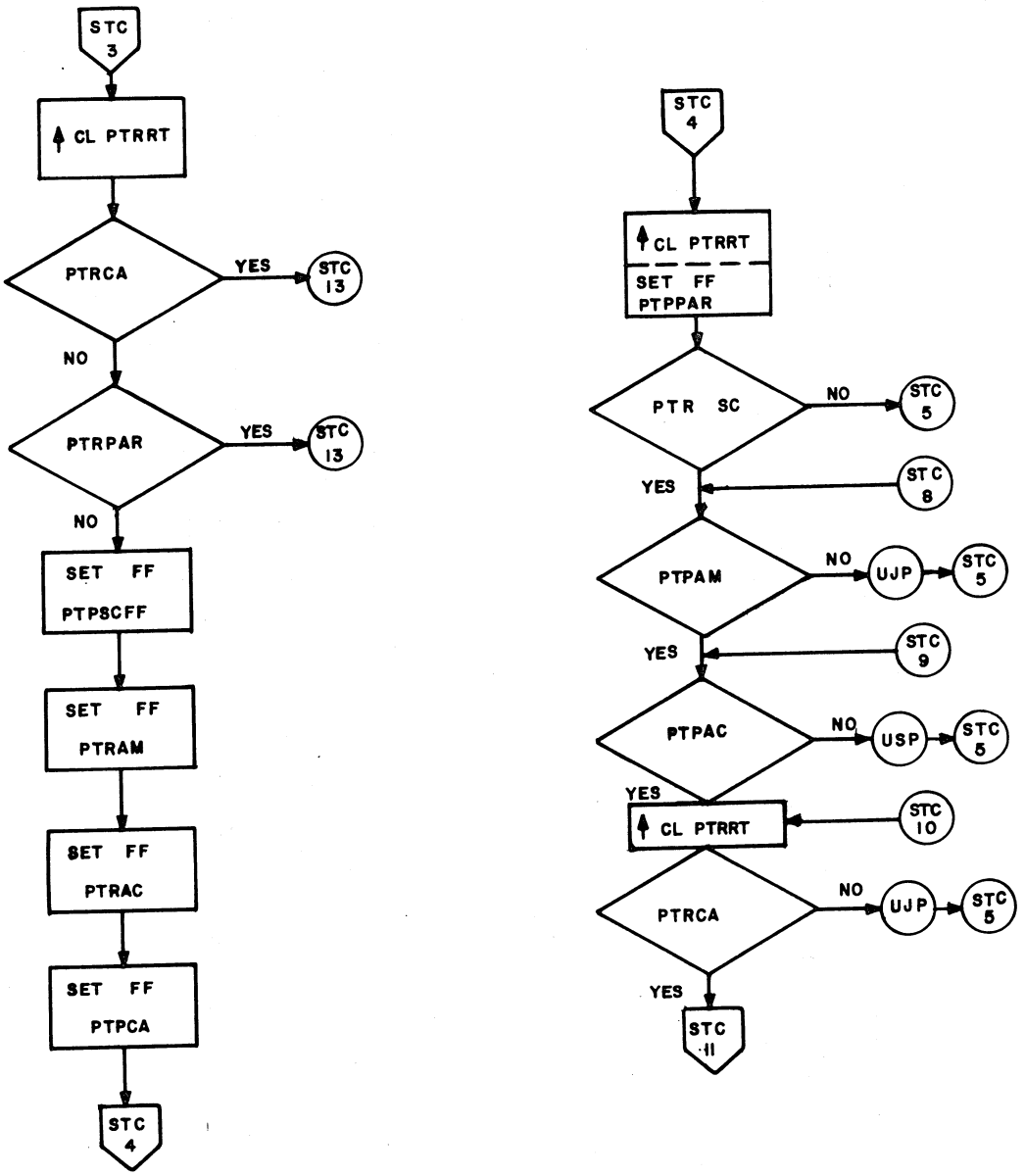
SELF TEST 2 (CONTINUED)



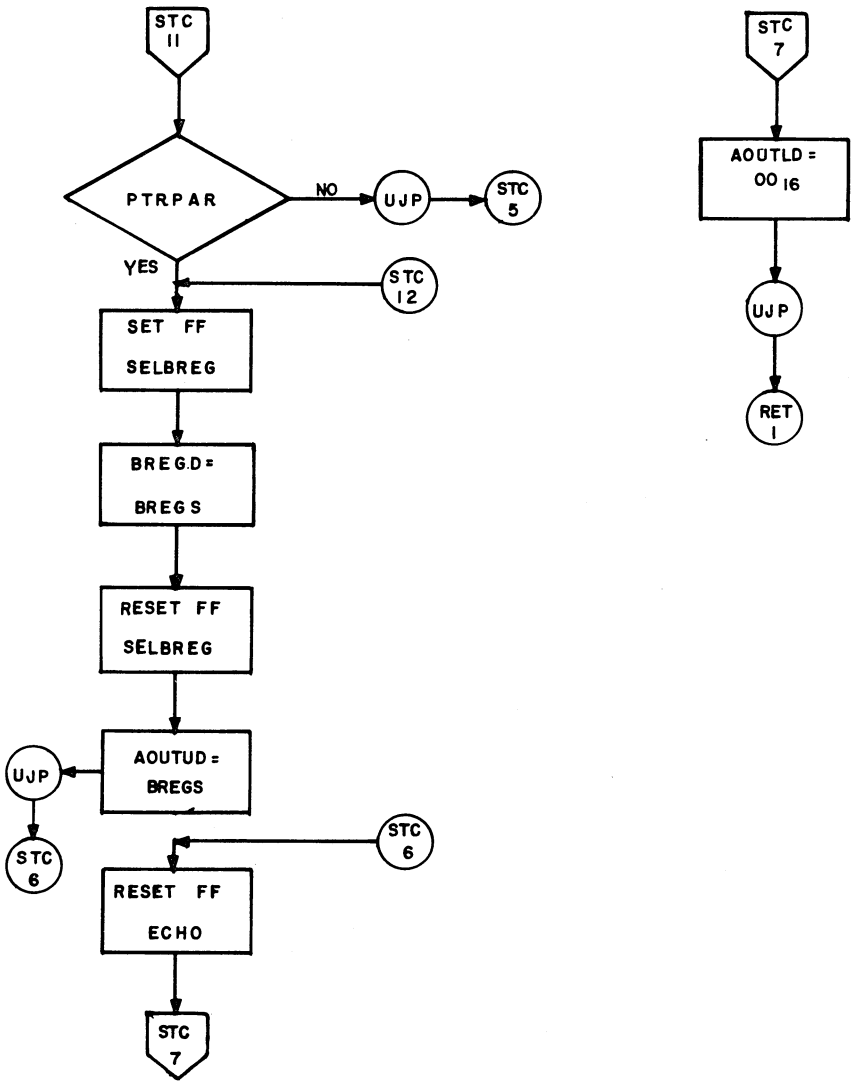
SELF TEST 2 (CONTINUED)



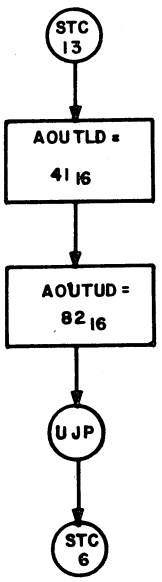
SELF TEST 3 A/Q COMMAND

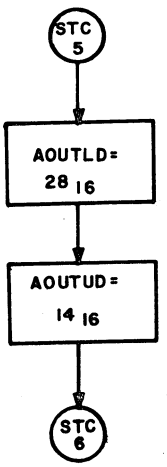


SELF TEST 3 (CONTINUED)

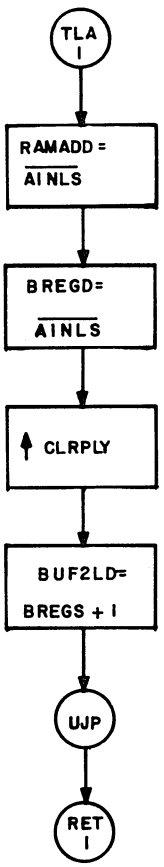


SELF TEST 3 (CONTINUED)

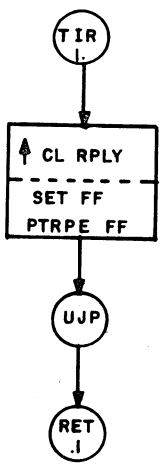




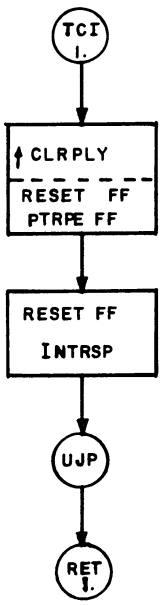
SELF TEST 3 (CONTINUED)



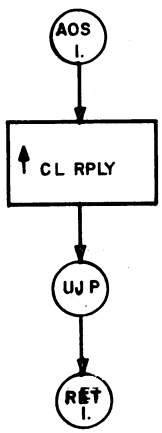
TEST MODE LOAD RAM ADDRESS A/Q COMMAND



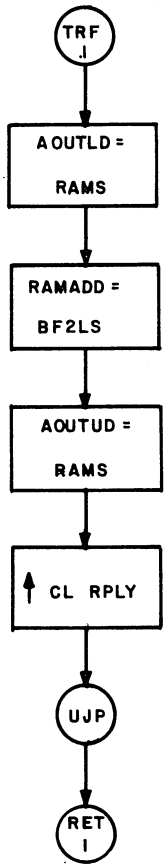
TEST MODE INTERRUPT REQUEST A/Q COMMAND



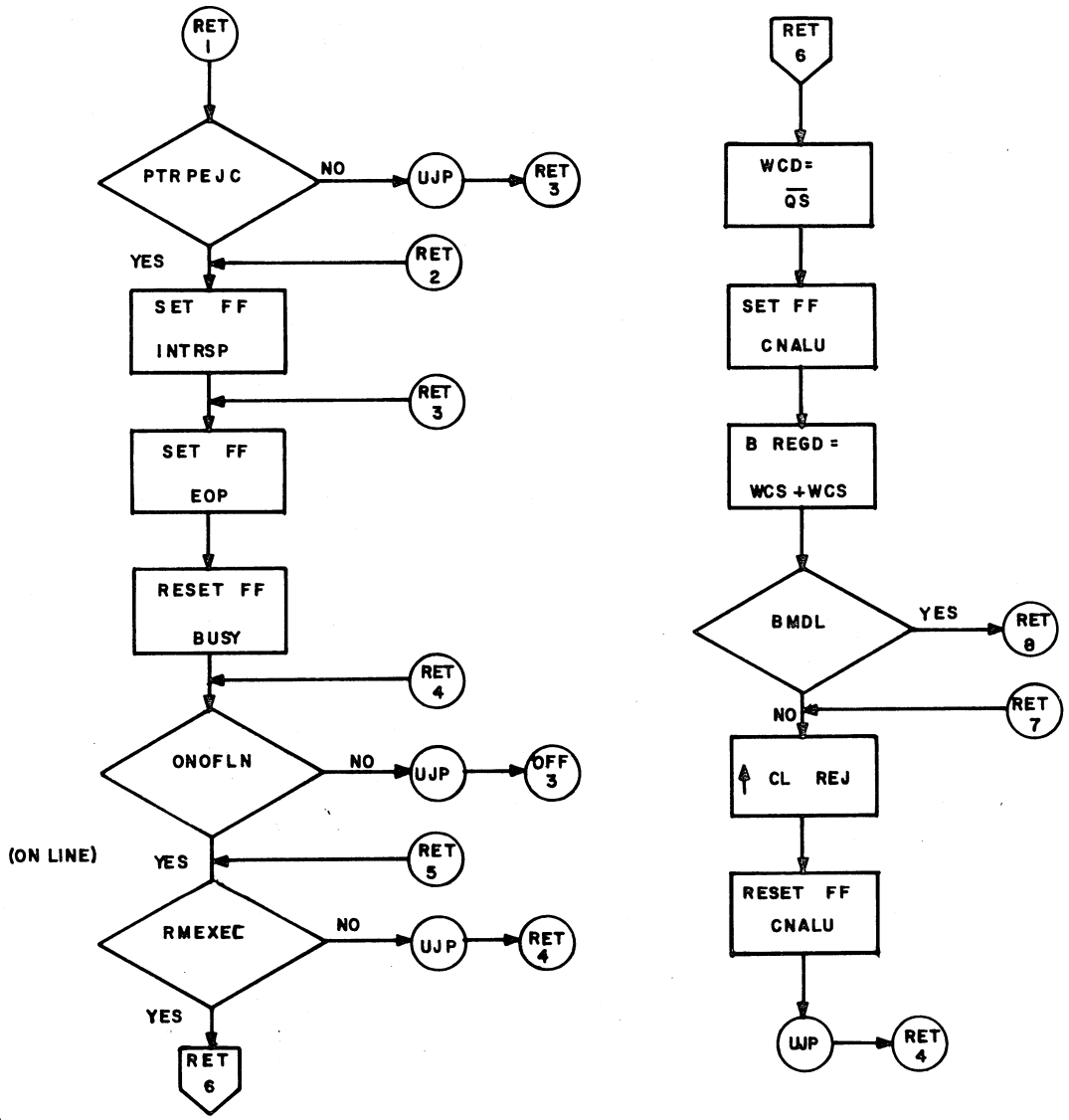
TEST MODE CLEAR INTERRUPT A/Q COMMAND



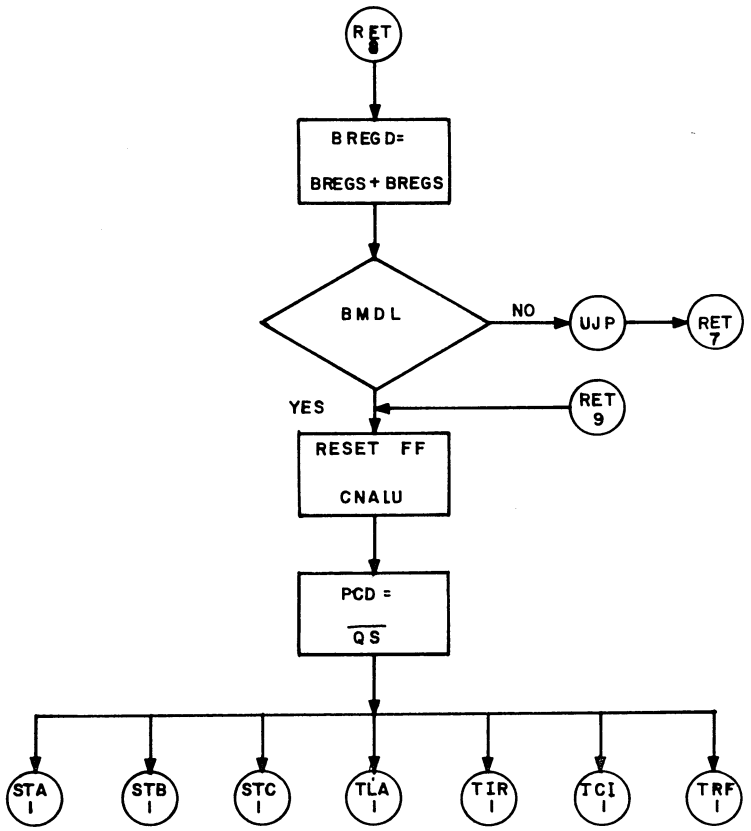
TEST MODE A-OUT STATUS A/Q COMMAND



TEST MODE READ RAM A/Q COMMAND



TEST MODE A/Q COMMAND HANDLING



TEST MODE A/Q COMMAND . HANDLING

PROGRAM LISTING

```
FE516A              PAGE   1              DATE: 06/05/77

0001                    NAM FE516A
0002              *
0003              *
0004              *
0005              ************************************************************
0006              ************************************************************
0007              **                                                        **
0008              **                    MICRO-PROGRAM ASSEMBLER             **
0009              **                                                        **
0010              **   PAPER TAPE READER/PAPER TAPE PUNCH/CARD PUNCH CONTROLLER **
0011              **                          FE516-A                       **
0012              **                                                        **
0013              **                      89601267  REV-01                **
0014              **                                                        **
0015              ************************************************************
0016              ************************************************************
0017              *
0018              *
0019              *
0020              *                        **** MACROS DEFINITIONS ****
0021              *
0022              *
0023              *
0024              CJP     MAC     JC,JA           CONDITIONAL JUMP-IF 'JC' GO TO 'JA'
0025                      VFD     N1/0,X6/'JC',X9/'JA'-START1
0026                      EMC
0027              UJP     MAC     JA                      UNCONDITIONAL JUMP-GO TO 'JA'
0028                      VFD     N7/0,X9/'JA'-START1
0029                      EMC
0030              LDC     MAC     D,C                     LOAD CONSTANT-LOAD 'D' BY 'C'
0031                      VFD     N4/$8,X4/'D',X8/'C'
0032                      EMC
0033              LADDR   MAC     D,AD                    LOAD ADDRESS-LOAD 'D' BY
0034              *                                           VALUE OF LABEL 'AD'
0035                      VFD     N4/$8,X4/'D',X8/'AD'-START1
0036                      EMC
0037              SFFCL   MAC     FF,CL                   SET FLIP FLOP & CONTROL LINE
0038              *                                  SET 'FF' & PROVIDE  PULSE ON 'CL'
0039                      VFD     N4/$8,X4/'CL',N2/0,X6/'FF'
0040                      EMC
0041              *
0042              *
0043              *
0044              *
0045              *
0046              *
0047              *
0048              *
0049              *
0050              *
0051              *
0052              *
0053              *
```

```
0054          RFFCL  MAC    FF,CL                    RESET FLIP-FLOP & CONTROL LINE
0055          *                                RESET 'FF' & PROVIDE  PULSE ON 'CL'
0056                 VFD    N4/$A,X4/'CL',N2/0,X6/'FF'
0057                 EMC
0058          CLO    MAC    CL                       CONTROL LINE (ONLY)-
0059          *                                            PROVIDE  PULSE ON 'CL'
0060                 VFD    N4/$B,X4/'CL',N8/$FF
0061                 EMC
0062          SFF    MAC    FF                       SET FLIP FLOP-SET 'FF'
0063                 VFD    N10/$2FC,X6/'FF'
0064                 EMC
0065          RFF    MAC    FF                       RESET FLIP FLOP-RESET 'FF'
0066                 VFD    N10/$2BC,X6/'FF'
0067                 EMC
0068          *
0069          *
0070          *
0071          *                          ** INTER REGISTER LOGICAL FUNCTIONS **
0072          *
0073          TA     MAC    SA,D                     TRANSFER A:    SA--->D
0074                 VFD    N4/$C,X4/'D',N5/$1E,X3/'SA'
0075                 EMC
0076          CA     MAC    SA,D                     COMPLEMENT A:   SA/--->D
0077                 VFD    N4/$C,X4/'D',N5/$0,X3/'SA'
0078                  EMC
0079          TB     MAC    SB,D                     TRINSFER B:     SB--->D
0080                 VFD    N2/$3,X2/'SB',X4/'D',N8/$A0
0081                 EMC
0082          CB     MAC    SB,D                     COMPLEMENT B:  SB/--->D
0083                 VFD    N2/$3,X2/'SB',X4/'D',N8/$50
0084                 EMC
0085          CLEAR  MAC    D                        CLEAR      :   00--->D
0086                 VFD    N4/$F,X4/'D',N8/$35
0087                  EMC
0088          SETONE MAC    D                        SET TO ONE:    FF--->D
0089                 VFD    N4/$F,X4/'D',N8/$C5
0090                 EMC
0091          OR     MAC    SA,SB,D                  OR:   SA,OR,SB--->D
0092                 VFD    N2/$3,X2/'SB',X4/'D',N5/$1C,X3/'SA'
0093                 EMC
0094          *
0095          *
0096          *
0097          *
0098          *
0099          *
0100          *
0101          *
0102          *
0103          *
0104          *
0105          *
0106          *
```

```
0107            COR     MAC     SA,SB,D       COMPLEMENT OR (NOR):(SA.OR.SB)/--->D
0108                    VFD     N2/$3,X2/'SB',X4/'D',N5/$2,X3/'SA'
0109                    EMC
0110            ORCA    MAC     SA,SB,D          OR COMPLEMENT B: SA.OR.(SB/)--->D
0111                    VFD     N2/$3,X2/'SB',X4/'D',N5/$10,X3/'SA'
0112                    EMC
0113            ORCB    MAC     SA,SB,D          OR COMPLEMENT A: (SA/).OR.SB--->D
0114                    VFD     N2/$3,X2/'SB',X4/'D',N5/$1A,X3/'SA'
0115                    EMC
0116            XOR     MAC     SA,SB,D                EXCLUSIVE OR:  SA.XOR.SB--->D
0117                    VFD     N2/$3,X2/'SB',X4/'D',N5/$C,X3/'SA'
0118                    EMC
0119            CXOR    MAC     SA,SB,D                 COMPLEMENT EXCLUSIVE OR:
0120            *                                             (SA.XOR.SB)/--->D
0121                    VFD     N2/$3,X2/'SB',X4/'D',N5/$12,X3/'SA'
0122                    EMC
0123            ANDAB   MAC     SA,SB,D                 AND A B:   SA.AND.SB--->D
0124                    VFD     N2/$3,X2/''SB',X4/'D',N5/$16,X3/'SA'
0125                    EMC
0126            CAND    MAC     SA,SB,D                 COMPLEMENT AND (NAND):
0127            *                                             (SA.AND.SB)/--->D
0128                    VFD     N2/$3,X2/'SB',X4/'D',N5/$B,X3/'SA'
0129                    EMC
0130            ANDCA   MAC     SA,SB,D       AND COMPLEMENT A: (SA/).AND.SB--->D
0131                    VFD     N2/$3,X2/'SB',X4/'D',N5/$4,X3/'SA'
0132                    EMC
0133            ANDCB   MAC     SA,SB,D                 AND COMPLEMENT B:
0134            *                                              SA.AND.(SB/)--->D.
0135                    VFD     N2/$3,X2/'SB',X4/'D',N5/$E,X3/'SA'
0136                    EMC
0137            *
0138            *
0139            *
0140            *                       ** INTER REGISTER ARITHMETIC OPERATIONS **
0141            *
0142            *                                FLIP-FLOP CN SHOULD
0143            *                                BE PROPERLY SET OR RESET
0144            *                               BEFORE AN ARITHMETIC OPERATION
0145            *                                IS EXECUTED.
0146            *
0147            *
0148            *
0149            *
0150            *
0151            *
0152            *
0153            *
0154            *
0155            *
0156            *
0157            *
0158            *
0159            *
```

```
0160            *
0161            IA      MAC     SA,D                    INCREMENT A:  SA+1--->D
0162            *                                       CONDITION  CN=1
0163                    VFD     N4/$C,X4/'D',N5/$1,X3/'SA'
0164                    EMC
0165            DA      MAC     SA,D                    DECREMENT A:  SA-1--->D
0166            *                                       CONDITION  CN=0
0167                    VFD     N4/$C,X4/'D',N5/$1F,X3/'SA'
0168                    EMC
0169            PLUS    MAC     SA,SB,D                 PLUS:   SA+SB--->D
0170            *                                       CONDITION  CN=0
0171                    VFD     N2/$3,X2/'SB',X4/'D',N5/$13,X3/'SA'
0172                    EMC
0173            MINUS   MAC     SA,SB,D                 MINUS:  SA-SB--->D
0174            *                                       CONDITION  CN=1
0175                    VFD     N2/$3,X2/'SB',X4/'D',N5/$D,X3/'SA'
0176                    EMC
0177            PLUSI   MAC     SA,SB,D                 PLUS INCREMENT:  SA+SB+1--->D
0178            *                                       CONDITION  CN=1
0179                    VFD     N2/$3,X2/'SB',X4/'D',N5/$13,X3/'SA'
0180                    EMC
0181            LSFT    MAC     SA,D                    LEFT SHIFT:   SA+SA--->D
0182            *                                       CONDITION  CN=0
0183                    VFD     N4/$C,X4/'D',N5/$19,X3/'SA'
0184                     EMC
0185            LSFTI   MAC     SA,D            LEFT SHIFT INCREMENT: SA+SA+1--->D
0186            *                                       CONDITION  CN=1
0187                    VFD     N4/$C,X4/'D',N5/$19,X3/'SA'
0188                    EMC
0189            COMPR   MAC     SA,SB                   COMPR:    SA=SB ?
0190            *                                       CONDITION  CN=0
0191            *                                       THE RESULT IS SENSED ON THE
0192            *                                  A=B PIN OF THE ALU. THE DESTINATION
0193            *                                       IS AN UNUSED REGISTER:
0194            *                                       THEREFORE DATA REMAINS
0195            *                                       UNCHANGED
0196            *
0197            *
0198            *
0199            *
0200            *
0201            *
0202            *
0203            *
0204            *
0205            *
0206            *
0207            *
0208            *
0209            *
0210             *
0211            *
0212            *
```

```
0213                    VFD     N22/$3,X2/'SB',N9/$6D,X3/'SA'
0214                    EMC
0215            *
0216            IRAR    MAC     M,SA,SB,D       INTER REGISTER ARITHMETIC (GENERAL)
0217            *                                     THIS INSTRUCTION COVERS ALL 16
0218            *                                       AVAILABLE MODES OF ARITHMETIC
0219            *                                       OPERATIONS. ALL 16 MODES
0220            *                                       DEPEND ON THE STATE OF
0221            *                                       THE CN FLIP-FLOP.
0222            *                                       REFFER TO IRAR MODE DEF.
0223            *
0224            *                                       'M' IS THE MODE SYMBOL
0225            *
0226                    VFD     N2/$3,X2/'SB',X4/'D',X4/'M',N1/$1,X3/'SA'
0227                    EMC
0228            *
0229            NOOP    MAC
0230            *                                       NO OPERATION
0231                    VFD     N16/$BFFF
0232                    EMC
0233            SPARE   MAC
0234            *                                       SPARE-
0235            *                               PROM WORD REMAINS UNBURNED
0236                    VFD     N16/$FFFF
0237                    EMC
0238            *
0239            *
0240            *
0241            *                                  **** IRAR  MODE DEFINITIONS ****
0242            *
0243    0000            EQU     MODE0($0)               MODE0: SA+/+CN--->D
0244    0001            EQU     MODE1($1)               MODE1: (SA.OR.SB)+CN--->D
0245    0002            EQU     MODE2($2)               MODE2: (SA.OR.(SB/))+CN--->D
0246    0003            EQU     MODE3($3)               MODE3: FFFF+CN--->D
0247    0004            EQU     MODE4($4)          MODE4: SA+(SA.AND.(SB/))+CN--->D
0248    0005            EQU     MODE5($5)               MODE5:
0249            *                                 (SA.OR.SB)+(SA.AND.(SB/)+CN--->D
0250    0006            EQU     MODE6($6)               MODE6: SA-SB-1+CN--->D
0251    0007            EQU     MODE7($7)              MODE7: (SA.AND.(SB/)-1+CN--->D
0252    0008            EQU     MODE8($8)               MODE8: SA+(SA.AND.SB)+CN--->D
0253    0009            EQU     MODE9($9)               MODE9: SA+SB+CN--->D
0254    000A            EQU     MODEA($A)               MODEA:
0255            *                                  (SA.OR.(SB/))+(SA.AND.SB)+CN--->D
0256    000B            EQU     MODEB($B)               MODEB:(SA.AND.SB)-1+CN--->D
0257    000C            EQU     MODEC($C)               MODEC: SA+SA+CN--->D
0258    000D            EQU     MODED($D)               MODED: (SA.AND.SB)+SA+CN--->D
0259    000E            EQU     MODEE($E)          MODEE: (SA.AND.(SB/))+SA+CN--->D
0260    000F            EQU     MODEF($F)               MODEF: SA-1+CN--->D
0261            *
0262            *               **** DESTINATION REGISTERS ****
0263            *
0264    0003            EQU     NU($3)                  NOT USED
0265    0004            EQU     RAMADD($4)              RAM ADDRESS
```

```
0265  0005        EQU   BANKD($5)          BANK
0266  0006        EQU   RAMD($6)           RAM
0267  0007        EQU   PCD($7)           PROGRAM COUNTER
0268  0008        EQU   WCD($8)           WRITE CHARACTER FOR PTP
0269  0009        EQU   AOUTUD($9)         A REGISTER OUTPUT UPPER BYTE
0270  000A        EQU   CWALD($A)          CP WRITE LOWER (4 BIT)
0271  000B        EQU   CWAUD($B)          CP WRITE UPPER (4 BIT)
0272  000C        EQU   AOUTLD($C)         A REGISTER OUTPUT LOWER BYTE
0273  000E        EQU   BF2UD($E)          BUFFER 2 UPPER
0274  000F        EQU   BREGD($F)          B REGISTER
0275  000D        EQU   BF2LD($D)          BUFFER 2 LOWER
0276              *
0277              *          **** SOURCE A REGISTERS ****
0278              *
0279  0000        EQU   RAMS($0)           RAM
0280  0001        EQU   WCS($1)            WRITE CHARACTER FOR PTP
0281  0002        EQU   AINLS($2)          A LINES INPUT LOWER BYTE
0282  0003        EQU   AINUS($3)          A LINES INPUT UPPER BYTE
0283  0004        EQU   BREGS($4)          B REGISTER
0284  0005        EQU   QS($5)             Q LINES
0285  0007        EQU   PCS($7)            PROGRAM COUNTER
0286              *
0287              *          **** SOURCE B REGISTERS ***
0288              *
0289  0000        EQU   CWALS($0)          CP WRITE LOWER (4 BIT)
0290  0001        EQU   CWAUS($1)          CP WRITE UPPER (4 BIT)
0291  0003        EQU   BF2US($3)          BUFFER 2 UPPER
0292  0002        EQU   BF2LS($2)          BUFFER 2 LOWER
0293              *
0294              *          **** CONTROL LINES ****
0295              *
0296  0001        EQU   REJ($1)            SET REJECT
0297  0003        EQU   RPLY($3)           SET REPLY
0298  0004        EQU   CPFIRT($4)         RESET CP FEED & INFO READY
0299  0006        EQU   CPINST($6)         SET CP INFO READY
0300  0007        EQU   PTRRT($7)          RESET & UP-DATE PTRPAR,PTRCA
0301  000C        EQU   PTPDYRT($C)        RESET PTP DISASSEMBLY MODE
0302  000E        EQU   CPFEST($E)         SET CP FEED
0303              *
0304              *          **** JUMP CONDITIONS ****
0305              *
0306  003A        EQU   PTRSO($3A)    JC52  PTR SOURCE OPERABLE
0307  0038        EQU   PTRSC($38)    JC53  PTR SOURCE CONTROL
0308  0022        EQU   PTRACJC($22)  JC66  PTR AC INDEX (JC)
0309  000E        EQU   PTRAYJC($0E)  JC10  PTR ASSEMBLY MODE (JC)
0310  002A        EQU   PTRDTJC($2A)  JC62  PTR DATA STATUS (JC)
0311  0032        EQU   PTRPAR($32)   JC56  PTR PARITY BIT
0312  0030        EQU   PTRCA($30)    JC57  PTR CONTROL AVAILABLE
0313  000C        EQU   PTRPEJC($0C)  JC11  PTR PARITY ERROR (JC)
0314  0026        EQU   PTRBFJC($26)  JC64  PTR B REGISTER FULL (JC)
0315  003C        EQU   PTPAO($3C)    JC51  PTP ACCCEPTOR OPERABLE
0316  003E        EQU   PTPAC($3E)    JC50  PTP ACCEPTOR CONTROL
0317  0036        EQU   PTPAM($36)    JC54  PTP ACCEPTOR MESSAGE
```

```
0319    001A        EQU   PTPSCJC($1A)    JC62   PTP SC INDEX (JC)
0320    0008        EQU   PTPSTJC($08)    JC13   PTP START MODE (JC)
0321    0016        EQU   PTPDYJC($16)    JC64   PTP DISASSEMBLY MODE (JC)
0322    001C        EQU   PTPDSJC($1C)    JC61   PTP DISASSEMBLY STATUS (JC)
0323    0020        EQU   PTPDTJC($20)    JC67   PTP DATA STATUS (JC)
0324    0012        EQU   PTPCOJC($12)    JC66   PTP CUT PROGRAM (JC)
0325    0021        EQU   CPBSY($21)      JC27   CP BUSY SIGNAL
00326   0029        EQU   CPINFJC($29)    JC23   CP INFO READY(JC)
0327    0035        EQU   CPECER($35)     JC75   CP ECHO ERROR
0328    0039        EQU   CPPUIH($39)     JC73   CP PUNCH INHIBIT
0329    002F        EQU   CPRDY($2F)      JC20   CP READY
0330    003D        EQU   CPSTBY($3D)     JC71   CP STANDBY
0331    0037        EQU   CPHOER($37)     JC74   CP HOPPER EMPTY
0332    0025        EQU   CPFEDJC($25)    JC25   CP FEED (JC)
0333    0010        EQU   CPDATJC($10)    JC87   CP DATA STATUS (JC)
0334    0034        EQU   PARLTC($34)     JC55   PARITY LATCHED
0335    000A        EQU   PTPIRJC($0A)    JC12   PTP INFO READY (JC)
0336    001B        EQU   WCEMPT($1B)     JC83   WORD COUNTER EMPTY (COMP)
0337    0023        EQU   ONOFLN($23)     JC26   ON/OFF LINE SWITCH
0338    0004        EQU   MSW1($04)       JC95   MAINTENANCE SWITCH 1
0339    000A        EQU   MSW2($0A)       JC92   MAINTENANCE SWITCH 2
0340    0008        EQU   MSW3($08)       JC93   MAINTENANCE SWITCH 3
0341    000D        EQU   COUT($0D)       JC41   CARRY OUT (COMP)
0342    0028        EQU   BMSB($28)       JC63   B REGISTER BIT 2**7
0343    0014        EQU   BMDL($14)       JC85   B REGISTER BIT 2**5
0344    001E        EQU   ONBUSJC($1E)    JC80   ENABLE BUS TO DEVICES (JC)
0345    0024        EQU   UNITPRT($24)    JC65   UNITS PROTECTED
0346    000F        EQU   EQUAL($0F)      JC40   ALU A=B
0347    0004        EQU   RMEXEC($04)     JC15   ROM EXEC
0348            *
0349            *           **** FLIP-FLOPS ****
0350            *
0351    0021        EQU   PTRAC($21)      FF66   PTR ACCEPTOR CONTROL
0352    0001        EQU   PTRACFF($01)    FF76   PTR AC INDEX (FF)
0353    0025        EQU   PTRAM($25)      FF62   PTR ACCEPTOR MESSAGE
0354    000C        EEQU  PTRAYFF($0C)    FF53   PTR ASSEMBLY MODE (FF)
0355    002F        EQU   PTRDTFF($2F)    FF40   PTR DATA STATUS (FF)
0356    0009        EQU   PTRPEFF($09)    FF56   PTR PARITY ERROR (FF)
0357    0006        EQU   PTRBFFF($06)    FF71   PTR B REGISTER FULL (FF)
0358    0024        EQU   PTPSCFF($24)    FF63   PTP SC INDEX (FF)
0359    0035        EQU   PTPCA($35)      FF12   PTP CONTROL AVAILABLE
0360    001C        EQU   PTPPAR($1C)     FF33   PTP PARITY BIT
0361    000A        EQU   PTPSTFF($0A)    FF55   PTP START MODE (FF)
0362    0032        EQU   PTPDSFF($32)    FF15   PTP DISASSEMBLY STATUS (FF)
0363    0005        EQU   PTPDYFF($05)    FF72   PTP DISASSEMBLY MODE (FF)
0364    0002        EQU   PTPDTFF($02)    FF75   PTP DATA/FUNCTION STATUS
0365    0008        EQU   PTPIRFF($08)    FF57   PTP INFO READY (FF)
0366    0034        EQU   PTPCOFF($34)    FF13   PTP CUT PROGRAM (FF)
0367    0014        EQU   CPOFFS($14)     FF23   CP OFFSET
0368    0030        EQU   CPDATFF($30)    FF17   CP DATA STATUS (FF)
0369    0020        EQU   CNALU($20)      FF67   CN ALU
0370    0033        EQU   RMBNKS($33)     FF14   ROM BANK SELECT
0371    002D        EQU   SELBREG($2D)    FF42   SELECT B REGISTER
```

```
0372  0019        EQU   ENDLCK($19)     FF36   ENABLE DELAY CLOCK
0373  0023        EQU   OBSUSEF($23)    FF64   ENABLE BUS TO DEVICES (FF)
0374  001B        EQU   ENDLOP($1B)     FF34   ENABLE DELAY OPERATION
0375  001A        EQU   PARSUP($1A)     FF37   PARITY SUPPLEMENT
0376  002E        EQU   BUSY($2E)       FF41   CONTROLLER BUSY
0377  0029        EQU   JGRP9($29)      FF46   JUMP CONDITION ON GROUP 9 FF
0378  0028        EQU   INTRSP($28)     FF47   INTERRUPT RESPONSE
0379  0000        EQU   CNTPRT($00)     FF77   CONTROLLER PROTECT
0380  0003        EQU   EOP($03)        FF74   END OF OPERATION
0381  0031        EQU   ECHO($31)       FF16   ECHO
0382              ENT    START1

0384        *           *** ROUTINE NAME LABEL ABBREVIATIONS ***

0386        *           AOS       TEST MODE A-OUT STAATUS A/Q COMMAND
0387        *           CCI       CP CLEAR INTERRUPT A/Q COMMAND
0388        *           CCL       CP CLEAR A/Q COMMAND
0389        *           CDT       CP DATA A/Q COMMAND
0390        *           CFD       CP FEED A/Q COMMAND
0391        *           CIQ       CP INTERRUPT REQUEST A/Q COMMAND
0392        *           CLC       CLEAR CONTROLLER A/Q COMMAND AND INTERNAL
0393        *           COF       CP OFFSET A/Q COMMAND
0394        *           CS2       CP STATUS 2 A/Q COMMAND
0395        *           CS3       CP STATUS 3 A/Q COMMAND
0396        *           CS4       CP STATUS 4 A/Q COMMAND
0397        *           CS5       CP STATUS 5 A/Q COMMAND
0398        *           DLY       DELAY, INTERNAL
0399        *           IAC       SET PTR AC, INTERNAL
0400        *           ICD       SET CP DATA STATUS, INTERNAL
0401        *           ICI       CP INTERRUPT, INTERNAL
0402        *           ICM       COMMON INTERRUPT, INTERNAL
0403        *           ICR       CP READY STATUS, INTERNAL
0404        *           IPD       SET PTP DATA STATUS, INTERNAL
0405        *           IPI       PTP INTERRUPT, INTERNAL
0406        *           IPR       PTP READY STATUS, INTERNAL
0407        *           IPS       SET PTP SC, INTERNAL
0408        *           IRH       PTR CHARACTER HANDLING, INTERNAL
0409        *           IRI       PTR INTERRUPT, INTERNAL
0410        *           IRR       PTR READY STATUS, INTERNAL
0411        *           IRT       PTR CHARACTER TRANSFER, INTERNAL
0412        *           MLP       MAIN LOOP ENTRY POINT
0413        *           OCO       OFF-LINE CP ALL ONES PUNCHING
0414        *           OCT       OFF-LINE CP TRIANGLE PUNCHING
0415        *           OFF       SELECT OFF-LINE MAINTENANCE ROUTINE, INT.
0416        *           OPP       OFF-LINE PTP TRIANGLE PUNCHING
0417        *           ORB       OFF-LINE PTP BACKWARD MOTION
```

0419 * *** ROUTINE NAME LABEL ABBREVIATIONS (CONT.) ***

0421	*	ORF	OFF-LINE PTR FORWARD MOTION
0422	*	PCI	PTP CLEAR INTERRUPT A/Q COMMAND
0423	*	PCL	PTP CLEAR A/Q COMMAND
0424	*	PDF	PTP DEVICE FUNCTION A/Q COMMAND
0425	*	PDM	PTP DATA MODE A/Q COMMAND
0426	*	PDS	PTP DISASSY TRANSFER STATUS A/Q COMMAND
0427	*	PDT	PTP DATA A/Q COMMAND
0428	*	PIQ	PTP INTERRUPT REQUEST A/Q COMMAND
0429	*	PST	PTP STOP-START A/Q COMMAND
0430	*	RAL	PTR ALARM STATUS A/Q COMMAND
0431	*	RAS	PTR ASSY TRANSFER STATUS A/Q COMMAND
0432	*	RCI	PTR CLEAR INTERRUPT A/Q COMMAND
0433	*	RCL	PTR CLEAR A/Q COMMAND
0434	*	RDM	PTR DATA MODE A/Q COMMAND
0435	*	RDT	PTR READ DATA A/Q COMMAND
0436	*	REJ	REJECT
0437	*	REP	REPLY
0438	*	RET	TEST MODE A/Q COMMAND HANDLING
0439	*	REX	ROM EXECUTION (Q-->PC)
0440	*	RFB	PTR FORWARD-BACKWARD A/Q COMMAND
0441	*	RIQ	PTR INTERRUPT REQUEST A/Q COMMAND
0442	*	RST	PTR STOP-START A/Q COMMAND
0443	*	STA	SELF TEST 1 A/Q COMMAND
0444	*	STB	SELF TEST 2 A/Q COMMAND
0445	*	STC	SELF TEST 3 A/Q COMMAND
0446	*	TCI	TEST MODE CLEAR INTERRUPT A/Q COMMAND
0447	*	TIR	TEST MODE INTERRUPT REQUEST A/Q COMMAND
0448	*	TLA	TEST MODE LOAD RAM ADDRESS A/Q COMMAND
0449	*	TRF	TEST MODE READ RAM A/Q COMMAND

```
0451              ***************************************************************
0452              *                                                             *
0453              *         THE LISTING INCLUDES THREE TYPES OF ROUTINES :      *
0454              *            -A/Q COMMAND HANDLING ROUTINES. REGULAR AND      *
0455              *             TEST MODE.                                      *
0456              *            -INTERNAL CONTROLLER DEVICE HANDLING ROUTINES.   *
0457              *            -OFF LINE MAINTENANCE ROUTINES.                 *
0458              *                                                            *
0459              *         THREE DEVICES ARE INVOLVED :                       *
0460              *            -PAPER TAPE READER  (PTR)                       *
0461              *            -PAPER TAPE PUNCH   (PTP)                       *
0462              *            -CARD PUNCH         (CP )                       *
0463              *                                                            *
0464              *         THE CONTROLLER COMMUNICATES WITH THE PAPER TAPE     *
0465              *         DEVICES VIA THE PT-RELAY STATION.                  *
0466              *                                                            *
0467              ***************************************************************


0469              ***************************************************************
0470              *       ALL PROGRAMS ASSUME THAT:                             *
0471              *        - FF42  SELHREG  IS NORMALLY RESET                   *
0472              *        - FF37  PARSUP   IS NORMALLY RESET                   *
0473              *        - FF67  CNALU    IS NORMALLY RESET                   *
0474              *       THEREFORE, AT THE END OF EACH PROGRAM THESE FF'S      *
0475              *        SHOULD HAVE THE ABOVE SPECIFIED VALUES.              *
0476              ***************************************************************
0477              START1 UJP    START2
0477 P0000 0001
0478              START2 UJP    CLC1
0478 P0001 005A
0479                     UJP    REJ1                 ILLEGAL (REJECT)
0479 P0002 0055
0480                     UJP    REJ1                 ILLEGAL (REJECT)
0480 P0003 0055
0481                     UJP    RDT1                 PTR READ DATA A/Q COMMAND
0481 P0004 0180
0482                     UJP    RAS1                 PTR ASSY TRANSFER STATUS
0482 P0005 0187
0483              *                                    A/Q COMMAND
0484                     UJP    RAL1                 PTR ALARM STATUS
0484 P0006 0190
0485              *                                    A/Q COMMAND
0486                     UJP    PDS1                 PTP DISASSY TRANSFER STATUS
0486 P0007 01D1
0487              *                                    A/Q COMMAND
0488                     UJP    CS21                 CP STATUS 2 A/Q COMMAND
0488 P0008 000C
```

```
0490                    UJP     CS31            CP STATUS 3 A/Q COMMAND
0490 P0009 0010
0491                    UJP     CS41            CP STATUS 4 A/Q COMMAND
0491 P000A 0014
0492                    UJP     CS51            CP STATUS 5 A/Q COMMAND
0492 P000B 0018


0494            ********************************************************************
0495            *                                                                  *
0496            *                  CP STATUS 2 A/Q COMMAND                         *
0497            *                                                                  *
0498            ********************************************************************


0500            CS21    LDC     AOUTLD,01
0500 P000C 8C01
0501                    CJP     CPPUIH,REP1
0501 P000D 7253
0502                    LDC     AOUTLD,00
0502 P000E 8C00
0503                    UJP     REP1
0503 P000F 0053


0505            ********************************************************************
0506            *                                                                  *
0507            *                  CP STATUS 3 A/Q COMMAND                         *
0508            *                                                                  *
0509            ********************************************************************


0511            CS31    LDC     AOUTLD,01
0511 P0010 8C01
0512                    CJP     CPECER,REP1
0512 P0011 6A53
0513                    LDC     AOUTLD,00
0513 P0012 8C00
0514                    UJP     REP1
0514 P0013 0053
```

```
0516              ********************************************************************
0517              *                                                                  *
0518              *                    CP STATUS 4 A/O COMMAND                       *
0519              *                                                                  *
0520              ********************************************************************


0522              CS41    LDC     AOUTLD,01
0522 P0014 8C01
0523                      CJP     CPSTBY,REP1
0523 P0015 7A53
0524                      LDC     AOUTLD,00
0524 P0016 8C00
0525                      UJP     REP1
0525 P0017 0053

0527              ********************************************************************
0528              *                                                                  *
0529              *                    CP STATUS 5 A/O COMMAND                       *
0530              *                                                                  *
0531              ********************************************************************


0533              CS51    LDC     AOUTLD,01
0533 P0018 8C01
0534                      CJP     CPHOEM,REP1
0534 P0019 6E53
0535                      LDC     AOUTLD,00
0535 P001A 8C00
0536                      UJP     REP1
0536 P001B 0053
0537                      UJP     REJ1                    ILLEGAL (REJECT)
0537 P001C 0055
0538                      UJP     REJ1                    ILLEGAL (REJECT)
0538 P001D 0055
0539                      UJP     AOS0                    A-OUT STATUS A/O COMMAND
0539 P001E 0042
0540                      UJP     TEM7                    TEST MODE READ FILE A/O COMM.
0540 P001F 0050
0541                      SPARE
0541 P0020 FFFF
0542                      SPARE
0542 P0021 FFFF
0543                      UJP     CFD1                    CP FEED  A/O COMMAND
0543 P0022 01D6
```

```
0545                    UJP     CCL1    CP CLEAR A/Q COMMAND
0545 P0023 01DD
0546                    UJP     CCI0    CP CLEAR INTERRUPT A/Q COMM.
0546 P0024 0040
0547                    UJP     CIQ1    CP INTERRUPT REQUEST A/Q COM.
0547 P0025 01E0
0548                    UJP     COF1    CP OFFSET A/Q COMMAND
0548 P0026 01E2
0549                    UJP     CDT1    CP DATA A/Q COMMAND
0549 P0027 01E7
0550                    UJP     RST1    PTR STOP-START A/Q COMMAND
0550 P0028 0145
0551                    UJP     RFB1    PTR FORWOARD-BACKWARD A/Q COM.
0551 P0029 014E
0552                    UJP     RCL1    PTR CLEAR A/Q COMMAND
0552 P002A 015E
0553                    UJP     RCI1    PTR CLEAR INTERRUPT A/Q COMM.
0553 P002B 016F
0554                    UJP     RIQ1    PTR INTERRUPT REQUEST A/Q COM
0554 P002C 017C
0555                    UJP     RDM1    PTR DATA MODE A/Q COMMAND
0555 P002D 0156
0556                    UJP     REJ1    ILLEGAL (REJECT)
0556 P002E 0055
0557                    UJP     REJ1    ILLEGAL (REJECT)
0557 P002F 0055
0558                    UJP     PST1    PTP STOP-START A/Q COMMAND
0558 P0030 0195
0559                    UJP     PDF1    PTP DEVICE FUNCTION A/Q COMM.
0559 P0031 01C4
0560                    UJP     PDT1    PTP DATA  A/Q COMMAND
0560 P0032 01B8
0561                    UJP     PCL1    PTP CLEAR A/Q COMMAND
0561 P0033 01A1
0562                    UJP     PCI1    PTP CLEAR INTERRUPT A/Q COMM.
0562 P0034 01AD
0563                    UJP     PIQ1    PTP INTERRUPT REQUEST A/Q COM
0563 P0035 01B6
0564                    UJP     PDM1    PTP DATA MODE A/Q COMMAND
0564 P0036 0198
0565                    UJP     REJ1    ILLEGAL (REJECT)
0565 P0037 0055
0566                    UJP     TEM1    SELF TEST ONE  A/Q COMMAND
0566 P0038 0044
0567                    UJP     TEM2    SELF TEST TWO  A/Q COMMAND
0567 P0039 0046
0568                    UJP     TEM3    SELF TEST THREE A/Q COMMAND
0568 P003A 0048
0569                    UJP     TEM4    TEST MODE LOAD FILE ADDRESS
0569 P003B 004A                          A/Q COMMAND
0570                *
```

```
0572                        UJP   TEM5          TEST MODE INTERRUPT REQUEST
0572 P003C 004C
0573                  *                         A/Q COMMAND
0574                        UJP   TEM6          TEST MODE CLEAR INTERRUPT
0574 P003D 004E
0575                  *                         A/Q COMMAND
0576                        UJP   REJ1          ILLEGAL (REJECT)
0576 P003E 0055
0577                        UJP   REJ1          ILLEGAL (REJECT)
0577 P003F 0055
0578                  CCI0  SFF   RMBNKS
0578 P0040 BF33
0579                        UJP   CCI1
0579 P0041 0000
0580                  AOS0  SFF   RMBNKS
0580 P0042 BF33
0581                        UJP   AOS1
0581 P0043 016D
0582                  TEM1  SFF   RMBNKS
0582 P0044 BF33
0583                        UJP   STA1
0583 P0045 00B2
0584                  TEM2  SFF   RMBNKS
0584 P0046 BF33
0585                        UJP   STB1
0585 P0047 00CF
0586                  TEM3  SFF   RMBNKS
0586 P0048 BF33
0587                        UJP   STC1
0587 P0049 0138
0588                  TEM4  SFF   RMBNKS
0588 P004A BF33
0589                        UJP   TLA1
0589 P004B 0163
0590                  TEM5  SFF   RMBNKS
0590 P004C BF33
0591                        UJP   TIR1
0591 P004D 0168
0592                  TEM6  SFF   RMBNKS
0592 P004E BF33
0593                        UJP   TCI1
0593 P004F 016A
0594                  TEM7  SFF   RMBNKS
0594 P0050 BF33
0595                        UJP   TRF1
0595 P0051 016F
0596                  REX1  CA    QS*PCD
0596 P0052 C705
0597                  REP1  CLO   RPLY
0597 P0053 B3FF
0598                        UJP   MLP1
0598 P0054 0056
```

```
0600                    REJ1    CLO     REJ
0600 P0055 B1FF
0601                    ********************************************************************
0602                    *                                                                  *
0603                    *                  MAIN LOOP ENTRY POINT , INTERNAL                *
0604                    *                                                                  *
0605                    *       THIS POINT IS REACHED AFTER EVERY:                         *
0606                    *        - MASTER CLEAR                                            *
0607                    *        - CLEAR CONTROLLER                                        *
0608                    *        - A/Q COMMAND                                             *
0609                    *                                                                  *
0610                    ********************************************************************

0612                    MLP1    CJP     ONOFLN,MLP2             JUMP IF ON LINE
0612 P0056 4658
0613                            UJP     CLC1
0613 P0057 005A
0614                    MLP2    CJP     RMEXEC,REX1
0614 P0058 0852
0615                            UJP     ICM1
0615 P0059 0089

0617                    ********************************************************************
0618                    *                                                                  *
0619                    *           CLEAR CONTROLLER A/Q COMMAND AND INTERNAL              *
0620                    *                                                                  *
0621                    *       THIS POINT IS REACHED:                                     *
0622                    *        - AFTER EVERY MASTER CLEAR                                *
0623                    *        - AFTER EVERY A/Q CLEAR CONTROLLER COMMAND                *
0624                    *        - BEFORE AND AFTER ANY OFF-LINE ROUTINE IS EXECUTED       *
0625                    *                                                                  *
0626                    ********************************************************************

0628                    CLC1    SFF     BUSY
0628 P005A BF2E
0629                            CJP     RMEXEC,CLC11
0629 P005B 085D
0630                            UJP     CLC12
0630 P005C 005E
0631                    CLC11   CLO     RPLY
0631 P005D B3FF
0632                    CLC12   SFF     CNALU
0632 P005E BF20
0633                            RFF     RMBNKS
0633 P005F AF33
0634                            RFF     SELBREG
0634 P0060 AF2D
0635                            LDC     BREGD,$10
0635 P0061 8F10
0636                    CLC2    TA      BREGS,RAMADD
0636 P0062 C4F4
```

```
0638                        LDC     RAMD,00
0638 P0063 8600
0639                CLC3    DA      REGS,REED
0639 P0064 CFEC
0640                        CJP     COUT,CLC4
0640 P0065 1A67
0641                        JJP     CLC2
0641 P0066 0062
0642                CLC4    RFF     CNALU
0642 P0067 AF20
0643                        SFF     ONBUSFF
0643 P0068 8F23
0644                        SFF     CNTPRT
0644 P0069 8F00
0645                        CJP     UNTPRT,CLC6
0645 P006A 486C
0646                CLC5    RFF     CNTPRT
0646 P006B AF00
0647                CLC6    RFF     ECHO
0647 P006C AF31
0648                        RFF     ENDLOP
0648 P006D AF1B
0649                        RFF     ENDLCK
0649 P006E AF19
0650                        RFF     PARSUP
0650 P006F AF18
0651                        RFF     JGRP9
0651 P0070 AF29
0652                CLC7    RFF     INTRSP
0652 P0071 AF28
0653                        RFF     PTRPEFF
0653 P0072 AF09
0654                        RFF     PTRAC
0654 P0073 AF21
0655                        RFF     PTRACFF
0655 P0074 AF01
0656                        RFF     PTRAM
0656 P0075 AF25
0657                        RFF     PTRAYFF
0657 P0076 AF0C
0658                CLC8    RFF     PTRDTFF
0658 P0077 AF2F
0659                        RFF     PTRBFFF
0659 P0078 AF06
0660                        RFF     PTPSCFF
0660 P0079 AF24
0661                        RFF     PTPCA
0661 P007A AF35
0662                        RFF     PTPPAR
0662 P007B AF1C
0663                        RFF     PTPSTFF
0663 P007C AF0A
```

```
0665                    CLC9    RFF     PTPDYFF
0665 P007D AF05
0666                            RFF     PTPDSFF
0666 P007E AF32
0667                            RFF     PTPDTFF
0667 P007F AF02
0668                            RFF     PTPCUFF
0668 P0080 AF34
0669                            RFF     PTPIRFF
0669 P0081 AF08
0670                            RFF     CPOFFS
0670 P0082 AF14
0671                    CLC10   RFFCL   CPDATFF,CPFIRT
0671 P0083 A430
0672                            RFF     BUSY
0672 P0084 AF2E
0673                            RFF     EOP
0673 P0085 AF03
0674                            CJP     ONOFLN,MLP1
0674 P0086 4656
0675                            SFF     RMBNKS
0675 P0087 BF33
0676                            UJP     DLY1
0676 P0088 000E


0678                    ********************************************************************
0679                    *                                                                  *
0680                    *                    COMMON INTERRUPT , INTERNAL                   *
0681                    *                                                                  *
0682                    *        THIS PROGRAM CONTROLS THE INTERRUPT RESPONSE LINE         *
0683                    *                                                                  *
0684                    ********************************************************************


0686                    ICM1    LDC     RAMADD,1
0686 P0089 8401
0687                            TA      RAMS,BREGD
0687 P008A CFF0
0688                            CJP     BMSB,ICM4               JUMP IF PTR INTRPT RESPONSE
0688 P008B 5095
0689                            LDC     RAMADD,2
0689 P008C 8402
0690                            TA      RAMS,BREGD
0690 P008D CFF0
0691                            CJP     BMSB,ICM4               JUMP IF PTP INTRPT RESPONSE
0691 P008E 5095
0692                    ICM2    LDC     RAMADD,3
0692 P008F 8403
0693                            TA      RAMS,BREGD
0693 P0090 CFF0
```

```
0695                    CJP     BMSB,ICM4           JUMP IF CP INTRPT RESPONSE
0695 P0091 5095
0696                    RFF     INTRSP              RESET INTERRUPT RESPONSE
0696 P0092 BF28
0697                ICM3    CJP     RMEXEC,REX1     JUMP IF ROM EXEC
0697 P0093 0852
0698                    UJP     IAC1
0698 P0094 0097
0699                ICM4    SFF     INTRSP          SET INTERRUPT RESPONSE
0699 P0095 BF28
0700                    UJP     ICM3
0700 P0096 0093


0702                ********************************************************************
0703                *                                                                  *
0704                *                  SET PTR AC SIGNAL , INTERNAL                    *
0705                *                                                                  *
0706                ********************************************************************


0708                IAC1    CJP     PTRACJC,IAC5
0708 P0097 44A2
0709                    CJP     PTRDTJC,IAC5        JUMP IF PTR DATA STATUS
0709 P0098 54A2
0710                    LDC     RAMADD,7
0710 P0099 8407
0711                    TA      RAMS,BREGD
0711 P009A CFF0
0712                    CJP     BMSB,IAC2           JUMP IF PTR START MODE
0712 P009B 509D
0713                    UJP     IAC5
0713 P009C 00A2
0714                IAC2    CJP     PTRSO,IAC3
0714 P009D 749F
0715                    UJP     IAC5
0715 P009E 00A2
0716                IAC3    CJP     PTRSC,IAC5
0716 P009F 70A2
0717                IAC4    SFF     PTRAC
0717 P00A0 BF21
0718                    SFF     PTRACFF
0718 P00A1 BF01
0719                IAC5    CJP     RMEXEC,REX1
0719 P00A2 0852
0720                    UJP     IRT1
0720 P00A3 00A4
```

```
0722                ************************************************************************
0723                *                                                                      *
0724                *                PTR CHARACTER TRANSFER , INTERNAL                     *
0725                *                                                                      *
0726                ************************************************************************


0728                IRT1    CJP     PTRBFJC,IRT2            JUMP IF B REGISTER FULL
0728 P00A4 4CA6
0729                        CJP     PTRACJC,IRT3
0729 P00A5 44AB
0730                IRT2    CJP     RMEXEC,REX1
0730 P00A6 0852
0731                        UJP     IPH1
0731 P00A7 00B8
0732                IRT3    CJP     PTRSC,IRT4
0732 P00A8 70AA
0733                        UJP     IRT2
0733 P00A9 00A6
0734                IRT4    SFFCL   PARSUP,PTRPT            SET PARITY LATCHED,
0734 P00AA B71B
0735                *                                        RESET & UP-DATE PTRPAR,PTRCA
0736                        CJP     PTRPAR,IRT7
0736 P00AB B4AD
0737                IRT6    RFF     PARSUP
0737 P00AC AF18
0738                IRT7    SFF     SELBREG
0738 P00AD BF2D
0739                        TA      BREGS,BREGD
0739 P00AE CFF4
0740                        RFF     SELBREG
0740 P00AF AF2D
0741                        LDC     RAMADD,9
0741 P00B0 B409
0742                IRT8    TA      BREGS,RAMD
0742 P00B1 C6F4
0743                        CJP     PARLTC,IRT9
0743 P00B2 68B4
0744                        UJP     IRT10
0744 P00B3 00B5
0745                IRT9    SFF     PTRPEFF
0745 P00B4 BF09
0746                IRT10   SFF     PTRBFFF
0746 P00B5 BF06
0747                        RFF     PARSUP
0747 P00B6 AF18
0748                        UJP     IRT2
0748 P00B7 00A6
```

```
0750              ********************************************************************
0751              *                                                                  *
0752              *                PTR CHARACTER HANDLING - INTERNAL                 *
0753              *                                                                  *
0754              ********************************************************************


0756              IRH1    CJP     PTRBFJC,IRH2
0756 P00B8 4CBA
0757                      UJP     IRH7
0757 P00B9 00C7
0758              IRH2    LDC     RAMADD,8
0758 P00BA 8408
0759                      TA      RAMS,BREGD
0759 P00BB CFF0
0760                      CJP     PTRPEJC,IRH10
0760 P00BC 18D0
0761                      CJP     PTRAYJC,IRH8
0761 P00BD 1CC9
0762              IRH3    LDC     BF2UD,00
0762 P00BE 8E00
0763              IRH4    LDC     RAMADD,7
0763 P00BF 8407
0764                      TA      RAMS,BREGD
0764 P00C0 CFF0
0765                      CJP     BMSB,IRH5               JUMP IF PTR START MODE
0765 P00C1 50C3
0766                      UJP     IRH7
0766 P00C2 00C7
0767              IRH5    SFF     PTRDTFF
0767 P00C3 BF2F
0768              IRH6    RFF     PTRBFFF
0768 P00C4 AF06
0769                      RFF     PTRAC
0769 P00C5 AF21
0770                      RFF     PTRACFF
0770 P00C6 AF01
0771              IRH7    CJP     RMEXEC,REX1
0771 P00C7 0852
0772                      UJP     IRI1
0772 P00C8 00D5
0773              IRH8    CJP     BMSB,IRH9               JUMP IF PTR ASSEMBLY STATUS
0773 P00C9 50CE
0774                      LDC     RAMD,$80                SET PTR ASSEMBLY STATUS
0774 P00CA 8680
0775                      LDC     RAMADD,9
0775 P00CB 8409
0776                      TA      RAMS,BF2UD              TRANSFER PTR UPPER BYTE
0776 P00CC CEF0
0777                      UJP     IRH6
0777 P00CD 00C4
```

```
0779                    IRH9    LDC     RAMD,00             RESET PTR ASSEMBLY STATUS
0779 P00CE 8600
0780                            UJP     IRH4
0780 P00CF 00BF
0781                    IRH10   CJP     PTRAYJC,IRH11       JUMP IF PTR ASSEMBLY MODE
0781 P00D0 1CD2
0782                            UJP     IRH3
0782 P00D1 00BE
0783                    IRH11   CJP     RMSB,IRH9           JUMP IF PTR ASSEMBLY STATUS
0783 P00D2 50CE
0784                            LDC     RAMD,$80            SET PTR ASSEMBLY STATUS
0784 P00D3 8680
0785                            UJP     IRH4
0785 P00D4 00BF

0787                    ********************************************************************
0788                    *                                                                  *
0789                    *                    PTR INTERRUPT , INTERNAL                      *
0790                    *                                                                  *
0791                    ********************************************************************

0793                    IRI1    LDC     RAMADD,4
0793 P00D5 8404
0794                            TA      RAMS,BREGD
0794 P00D6 CFF0
0795                            CJP     PTRSO,IRI2
0795 P00D7 74D9
0796                            CJP     BMSB,IRI4           JUMP IF PTR NOT RDY INTRPT RQ
0796 P00D8 50DC
0797                    IRI2    CJP     PTRDTJC,IRI5
0797 P00D9 54E0
0798                    IRI3    CJP     RMEXEC,REX1
0798 P00DA 0852
0799                            UJP     IRD1
0799 P00DB 00E2
0800                    IRI4    LDC     RAMADD,1
0800 P00DC 8401
0801                            LDC     RAMD,$80            SET PTR INTERRUPT RESPONSE
0801 P00DD 8680
0802                            SFF     INTRSP
0802 P00DE BF28
0803                            UJP     IRI3
0803 P00DF 00DA
0804                    IRI5    CJP     BMDL,IRI4           JUMP IF PTR DATA INTRPT RQ
0804 P00E0 28DC
0805                            UJP     IRI3
0805 P00E1 00DA
```

```
0807                ********************************************************************
0808                *                                                                  *
0809                *          SET PTP DATA/FUNCTION STATUS , INTERNAL                 *
0810                *                                                                  *
0811                ********************************************************************


0813                IPD1    CJP     PTPSTJC,IPD3            JUMP IF PTP START MODE
0813 P00F2 10E5
0814                IPD2    CJP     PMEXEC,REX1
0814 P00E3 0852
0815                        UJP     IPS1
0815 P00F4 00F3
0816                IPD3    CJP     PTPAC,IPD5
0816 P00E5 7CE8
0817                IPD4    RFF     PTPSCFF
0817 P00E6 AF24
0818                        UJP     IPD2
0818 P00F7 00E3
0819                IPD5    CJP     PTPSCJC,IPD2
0819 P00E8 34E3
0820                        CJP     PTPAM,IPD7
0820 P00E9 6CEF
0821                        CJP     PTPIPJC,IPD2
0821 P00EA 14E3
0822                IPD6    LDC     RAMADD,$0A
0822 P00EB 840A
0823                        TA      RAMS,BREGD
0823 P00EC CFF0
0824                        CJP     BMSB,IPD2               JUMP IF PTP INDEX CA
0824 P00ED 50E3
0825                        CJP     PTPDYJC,IPD8
0825 P00EE 2CF1
0826                IPD7    SFF     PTPDTFF
0826 P00EF BF02
0827                        UJP     IPD2
0827 P00F0 00E3
0828                IPD8    CJP     PTPDSJC,IPD2
0828 P00F1 38E3
0829                        UJP     IPD7
0829 P00F2 00EF
```

```
0831              ********************************************************************
0832              *                                                                  *
0833              *                  SET PTP SC SIGNAL , INTERNAL                    *
0834              *                                                                  *
0835              ********************************************************************


0837              IPS1   CJP    PTPSTJC,IPS3          JUMP IF PTP START MODE
0837 P00F3 10F6
0838              IPS2   CJP    RMEXEC,REX1
0838 P00F4 0852
0839                     UJP    IPI1
0839? P00F5 0110
0840              IPS3   CJP    PTPAC,IPS4
0840 P00F6 7CF8
0841                     UJP    IPS2
0841 P00F7 00F4
0842              IPS4   CJP    PTPSCJC,IPS2
0842 P00F8 34F4
0843                     CJP    PTPIRJC,IPS7
0843 P00F9 1501
0844                     LDC    RAMADD,$0A
0844 P00FA 840A
0845                     TA     RAMS,BREGD
0845 P00FB CFF0
0846              IPS5   CJP    BMSB,IPS6             JUMP IF PTP INDEX CA
0846 P00FC 50FE
0847                     UJP    IPS2
0847 P00FD 00F4
0848              IPS6   LDC    RAMD,00               RESET PTP INDEX CA
0848 P00FE 8600
0849                     SFF    PTPSCFF
0849 P00FF BF24
0850                     UJP    IPS2
0850 P0100 00F4
0851              IPS7   CJP    PTPDYJC,IPS12
0851 P0101 2D0A
0852              IPS8   RFF    PTPIRFF
0852 P0102 AF08
0853                     LDC    RAMADD,$0C
0853 P0103 840C
0854              IPS9   TA     RAMS,WCD
0854 P0104 C8F0
0855                     SFF    PTPPAR
0855 P0105 BF1C
0856                     CJP    PARLTC,IPS11
0856 P0106 6908
0857              IPS10  RFF    PTPPAR
0857 P0107 AF1C
0858              IPS11  SFF    PTPSCFF
0858 P0108 BF24
```

```
0860                    UJP     IPS2
0860 P0109 90F4
0861            IPS12   CJP     PTPDSJC,IPS13
0861 P010A 390E
0862                    SFF     PTPDSFF
0862 P010B BF32
0863                    LDC     RAMADD,$0B
0863 P010C 840B
0864                    UJP     IPS9
0864 P010D 0104
0865            IPS13   RFF     PTPDSFF
0865 P010E AF32
0866                    UJP     IPS8
0866 P010F 0102


0868            ********************************************************************
0869            *                                                                  *
0870            *                    PTP INTERRUPT , INTERNAL                      *
0871            *                                                                  *
0872            ********************************************************************


0874            IPI1    LDC     RAMADD,5
0874 P0110 8405
0875                    TA      RAMS,BREGD
0875 P0111 CFF0
0876                    CJP     PTPAO,IPI2
0876 P0112 7914
0877                    CJP     BMSB,IPI4               JUMP IF PTP NOT RDY INTRPT RQ
0877 P0113 5117
0878            IPI2    CJP     PTPDTJC,IPI5
0878 P0114 411B
0879            IPI3    CJP     RMEXEC,REX1
0879 P0115 0852
0880                    UJP     ICD1
0880 P0116 011D
0881            IPI4    LDC     RAMADD,2
0881 P0117 8402
0882                    LDC     RAMD,$80                SET PTP INTERRUPT RESPONSE
0882 P0118 8680
0883                    SFF     INTRSP
0883 P0119 BF28
0884                    UJP     IPI3
0884 P011A 0115
0885            IPI5    CJP     BMDL,IPI4               JUMP IF PTP DATA INTRPT RQ
0885 P011B 2917
0886                    UJP     IPI3
0886 P011C 0115
```

```
0888                ************************************************************************
0889                *                                                                      *
0890                *                    SET CP DATA STATUS , INTERNAL                     *
0891                *                                                                      *
0892                ************************************************************************


0894                ICD1    CJP     CPRDY,ICD3
0894 P011D 5F20
0895                ICD2    CJP     RMEXEC,REX1
0895 P011E 0852
0896                        UJP     ICI1
0896 P011F 0127
0897                ICD3    CJP     CPPUTH,ICD2
0897 P0120 731E
0898                        CJP     CPINFJC,ICD2
0898 P0121 531E
0899                        CJP     CPFEDJC,ICD2
0899 P0122 4B1E
0900                        CJP     CPBSY,ICD4
0900 P0123 4325
0901                        UJP     ICD2
0901 P0124 011E
0902                ICD4    SFF     CPDATFF
0902 P0125 BF30
0903                        UJP     ICD2
0903 P0126 011E
0904                ************************************************************************
0905                *                                                                      *
0906                *                      CP INTERRUPT , INTERNAL                         *
0907                *                                                                      *
0908                ************************************************************************


0910                ICI1    LDC     RAMADD,6
0910 P0127 8406
0911                        TA      RAMS,BREGD
0911 P0128 CFF0
0912                        CJP     CPRDY,ICI2
0912 P0129 5F2B
0913                        CJP     RMSB,ICI4               JUMP IF CP NOT RDY INTRPT RQ
0913 P012A 512E
0914                ICI2    CJP     CPDATJC,ICI5
0914 P012B 2132
0915                ICI3    CJP     RMEXEC,REX1
0915 P012C 0852
0916                        UJP     IRR1
0916 P012D 0134
0917                ICI4    LDC     RAMADD,3
0917 P012E 8403
```

```
0919                    LDC     RAMD,$80        SET CP INTERRUPT RESPONSE
0919 P012F A6A0
0920                    SFF     INTRSP
0920 P0130 AF28
0921                    UJP     ICI3
0921 P0131 012C
0922                ICI5    CJP     RMDL,ICI4
0922 P0132 242E
0923                    UJP     ICI3
0923 P0133 012C
0924                ********************************************************************
0925                *                                                                  *
0926                *                  PTR READY STATUS , INTERNAL                     *
0927                *                                                                  *
0928                ********************************************************************


0930                IRR1    CJP     PTRS0,IRR2
0930 P0134 7538
0931                    RFF     PTPDTFF
0931 P0135 AF2F
0932                    RFF     PTRAC
0932 P0136 AF21
0933                    RFF     PTRACFF
0933 P0137 AF01
0934                IPR2    CJP     RMEXEC,REX1
0934 P0138 0852
0935                    UJP     IPR1
0935 P0139 013A


0937                ********************************************************************
0938                *                                                                  *
0939                *                  PTP READY STATUS , INTERNAL                     *
0940                *                                                                  *
0941                ********************************************************************


0943                IPR1    CJP     PTPA0,IPR2
0943 P013A 793D
0944                    RFF     PTPDTFF
0944 P013B AF02
0945                    RFF     PTPSCFF
0945 P013C AF24
0946                IPR2    CJP     RMEXEC,REX1
0946 P013D 0852
0947                    UJP     ICR1
0947 P013E 013F
```

```
0949                ********************************************************************
0950                *                                                                  *
0951                *                    CP READY STATUS , INTERNAL                    *
0952                *                                                                  *
0953                ********************************************************************


0955                ICR1    CJP     CPRDY,ICP4
0955 P013F 5F43
0956                ICR2    RFFCL   CPDATFF,CPFIRT          RESET CP DATA,RESET CP FEED
0956 P0140 A430
0957                *                                        AND CP INFO READY
0958                ICR3    CJP     RMEXEC,REX1
0958 P0141 0852
0959                        UJP     MLP1
0959 P0142 0056
0960                ICR4    CJP     CPPUIH,ICR2
0960 P0143 7340
0961                        UJP     ICR3
0961 P0144 0141


0963                ********************************************************************
0964                *                                                                  *
0965                *                  PTR STOP-START A/Q COMMAND                      *
0966                *                                                                  *
0967                ********************************************************************


0969                RST1    CA      AINLS,AREGD
0969 P0145 CF02
0970                        CLO     RPLY
0970 P0146 83FF
0971                        LDC     RAMADD,7
0971 P0147 8407
0972                        LDC     RAMD,$80                SET PTR START MODE
0972 P0148 8680
0973                        CJP     BMSB,MLP1
0973 P0149 5056
0974                        LDC     RAMD,00                 RESET PTR START MODE
0974 P014A 8600
0975                RST2    RFF     PTRAC
0975 P014B AF21
0976                        RFF     PTRACFF
0976 P014C AF01
0977                        UJP     MLP1
0977 P014D 0056
```

```
0979                ************************************************************
0980                *                                                          *
0981                *              PTR FORWARD-BACKWARD A/Q COMMAND            *
0982                *                                                          *
0983                ************************************************************

0985                RFB1    LDC     RAMADD,7
0985 P014E 8407
0986                        TA      RAMS,BREGD
0986 P014F CFF0
0987                        CJP     BMSB,REJ1           JUMP IF PTR START MODE
0987 P0150 5055
0988                        CA      AINLS,BREGD
0988 P0151 CF02
0989                        SFFCL   PTRAM,RPLY
0989 P0152 B325
0990                        CJP     BMDL,MLP1
0990 P0153 2856
0991                RFB2    RFF     PTRAM
0991 P0154 AF25
0992                        UJP     MLP1
0992 P0155 0056

0994                ************************************************************
0995                *                                                          *
0996                *                PTR DATA MODE A/Q COMMAND                 *
0997                *                                                          *
0998                ************************************************************

1000                RDM1    LDC     RAMADD,7
1000 P0156 8407
1001                        TA      RRAMS,BREGD
1001 P0157 CFF0
1002                        CJP     BMSB,REJ1           JUMP IF PTR START MODE
1002 P0158 5055
1003                        CA      AINLS,BREGD
1003 P0159 CF02
1004                        SFFCL   PTRAYFF,RPLY
1004 P015A B30C
1005                        CJP     BMSB,MLP1
1005 P015B 5056
1006                RDM2    RFF     PTRAYFF
1006 P015C AF0C
```

```
1008                        UJP     MLP1
1008 P015D 0056

1010                ********************************************************************
1011                *                                                                  *
1012                *                        PTR CLEAR A/Q COMMAND                     *
1013                *                                                                  *
1014                ********************************************************************

1016                RCL1    CA      AINLS,BREGD
1016 P015E CF02
1017                        CLO     RPLY
1017 P015F B3FF
1018                        CJP     BMDL,RCL2
1018 P0160 2963
1019                        CJP     BMSB,RCL3
1019 P0161 5164
1020                        UJP     MLP1
1020 P0162 0056
1021                RCL2    RFF     PTRPEFF
1021 P0163 AF09
1022                RCL3    RFF     PTRAC
1022 P0164 AF21
1023                        RFF     PTRACFF
1023 P0165 AF01
1024                        RFF     PTRAM
1024 P0166 AF25
1025                        LDC     RAMADD,7
1025 P0167 8407
1026                        LDC     RAMD,00             RESET PTR START MODE
1026 P0168 8600
1027                RCL4    RFF     PTRAYFF
1027 P0169 AF0C
1028                        LDC     RAMADD,8
1028 P016A 8408
1029                        LDC     RAMD,00             RESET PTR ASSEMBLY STATUS
1029 P016B 8600
1030                        RFF     PTRDTFF
1030 P016C AF2F
1031                        RFF     PTRBFFF
1031 P016D AF06
1032                        UJP     MLP1
1032 P016E 0056
```

```
1034                ********************************************************************
1035                *                                                                  *
1036                *              PTR CLEAR INTERRUPT A/Q COMMAND                     *
1037                *                                                                  *
1038                ********************************************************************


1040                RCI1    CLO     RPLY
1040 P016F B3FF
1041                        LDC     RAMADD,4
1041 P0170 8404
1042                        LDC     RAMD,00             RESET PTR INTERRUPT REQUEST
1042 P0171 8600
1043                *                                    FOR DATA AND FOR NOT READY
1044                        LDC     RAMADD,1
1044 P0172 8401
1045                        LDC     RAMD,00             RESET PTR INTERRUPT RESPONSE
1045 P0173 8600
1046                        LDC     RAMADD,2
1046 P0174 8402
1047                RCI2    TA      RAMS,BREGD
1047 P0175 CFF0
1048                        CJP     BMSB,MLP1
1048 P0176 5056
1049                RCI3    LDC     RAMADD,3
1049 P0177 8403
1050                        TA      RAMS,BREGD
1050 P0178 CFF0
1051                        CJP     BMSB,MLP1
1051 P0179 5056
1052                        RFF     INTRSP              RESET INTERRUPT RESPONSE
1052 P017A AF28
1053                        UJP     MLP1
1053 P017B 0056
1054                ********************************************************************
1055                *                                                                  *
1056                *              PTR INTERRUPT REQUEST A/Q COMMAND                   *
1057                *                                                                  *
1058                ********************************************************************


1060                RIQ1    LDC     RAMADD,4
1060 P017C 8404
1061                RIQ2    CA      AINLS,RAMD
1061 P017D C602
1062                        CLO     RPLY
1062 P017E B3FF
1063                        UJP     MLP1
1063 P017F 0056
```

```
1065                ********************************************************************
1066                *                                                                  *
1067                *                    PTR READ DATA A/Q COMMAND                     *
1068                *                                                                  *
1069                ********************************************************************


1071                RDT1    CJP     PTRDTJC,RDT2
1071 P0180 3582
1072                        UJP     REJ1
1072 P0181 0055
1073                RDT2    LDC     RAMADD,9
1073 P0182 9409
1074                        TA      RAMS,AOUTLD             TRANSFER PTR SECOND CHARACTER
1074 P0183 CCF0
1075                        TA      RF2US,AOUTUD            TRANSFER PTR FIRST CHARACTER
1075 P0184 F9A0
1076                        RFFCL   PTRDTFF,RPLY
1076 P0185 A32F
1077                        UJP     MLP1
1077 P0186 0056
1078                ********************************************************************
1079                *                                                                  *
1080                *            PTR ASSEMBLY TRANSFER STATUS A/Q COMMAND              *
1081                *                                                                  *
1082                ********************************************************************


1084                RAS1    LDC     RAMADD,8
1084 P0187 8408
1085                        TA      RAMS,BREGD
1085 P0188 CFF0
1086                        CJP     BMSB,RAS2               JUMP IF PTR ASSEMBLY MODE
1086 P0189 518D
1087                        LDC     AOUTLD,00
1087 P018A 8C00
1088                        CLO     RPLY
1088 P018B B3FF
1089                        UJP     MLP1
1089 P018C 0056
1090                RAS2    LDC     AOUTLD,01
1090 P018D 8C01
1091                        CLO     RPLY
1091 P018E B3FF
1092                        UJP     MLP1
1092 P018F 0056
```

```
1094              ********************************************************************
1095              *                                                                  *
1096              *                  PTR ALARM STATUS A/Q COMMAND                    *
1097              *                                                                  *
1098              ********************************************************************


1100              RAL1    LDC     AOUTLD,01
1100 P0190 8C01
1101                      CJP     PTRPEJC,RAL2        JUMP IF PTR PARITY ERROR
1101 P0191 1993
1102                      LDC     AOUTLD,00
1102 P0192 8C00
1103              RAL2    CLO     RPLY
1103 P0193 83FF
1104                      UJP     MLP1
1104 P0194 0056


1106              ********************************************************************
1107              *                                                                  *
1108              *                  PTP STOP-START A/Q COMMAND                      *
1109              *                                                                  *
1110              ********************************************************************


1112              PST1    CA      AINLS,BREGD
1112 P0195 CF02
1113                      SFFCL   PTPSTFF,RPLY
1113 P0196 830A
1114                       CJP    BMSB,MLP1           JUMP IF PTP START MODE
1114 P0197 5056
1115                      RFF     PTPSTFF
1115 P0198 AF0A
1116                      RFF     PTPSCFF
1116 P0199 AF24
1117                      UJP     MLP1
1117 P019A 0056
```

```
1119                ********************************************************************
1120                *                                                                  *
1121                *                    PTP DATA MODE A/Q COMMAND                     *
1122                *                                                                  *
1123                ********************************************************************

1125                PDM1    CJP     PTPSTJC,FFJ1        JUMP IF START MODE
1125 P019E 1055
1126                        CA      AINLS,BREGD
1126 P019C CF02
1127                        SFFCL   PTPDYFF,RPLY
1127 P019D 3305
1128                        CJP     RMSR,MLP1
1128 P019E 5056
1129                        RFF     PTPDYFF
1129 P019F AF05
1130                        UJP     MLP1
1130 P01A0 1056

1132                ********************************************************************
1133                *                                                                  *
1134                *                    PTP CLEAR A/Q COMMAND                         *
1135                *                                                                  *
1136                ********************************************************************


1138                PCL1    RFFCL   PTPSCFF,RPLY
1138 P01A1 A324
1139                        RFF     PTPCA
1139 P01A2 AF35
1140                        RFF     PTPPAR
1140 P01A3 AF1C
1141                        RFF     PTPSTFF
1141 P01A4 AF0A
1142                        RFF     PTPDYFF
1142 P01A5 AF05
1143                        RFF     PTPDSFF
1143 P01A6 AF32
1144                        RFF     PTPDTFF
1144 P01A7 AF02
1145                PCL2    RFF     PTPCHFF
1145 P01A8 AF34
1146                        RFF     PTPIRFF
1146 P01A9 AF08
1147                        LDC     RAMADD,$0A
1147 P01AA B40A
```

```
1149                    LDC     RAMD,00
1149 P01AB 8600
1150                    UJP     NLP1
1150 P01AC 0056


1152            ********************************************************************
1153            *                                                                  *
1154            *                PTP CLEAR INTERRUPT A/Q COMMAND                   *
1155            *                                                                  *
1156            ********************************************************************


1158            PCI1    CLO     RPLY
1158 P01AD 83FF
1159                    LDC     RAMADD,5
1159 P01AE 8405
1160                    LDC     RAMD,00         RESET PTP INTERRUPT REQUEST
1160 P01AF 8600
1161            *                                 FOR DATA AND FOR NOT READY
1162                    LDC     RAMADD,2
1162 P01B0 8402
1163                    LDC     RAMD,00         RESET PTP INTERRUPT RESPONSE
1163 P01B1 8600
1164                    LDC     RAMADD,1
1164 P01B2 8401
1165            PCI2    TA      RAMS,BREGD
1165 P01B3 CFF0
1166                    CJP     BMSB,MLP1       JUMP IF PTR INTRPT RESPONSE
1166 P01B4 5056
1167                    UJP     RCI3
1167 P01B5 0177
1168            ********************************************************************
1169            *                                                                  *
1170            *            PTP INTERRUPT REQUEST A/Q COMMAND                     *
1171            *                                                                  *
1172            ********************************************************************


1174            PIQ1    LDC     RAMADD,5
1174 P01B6 8405
1175                    UJP     PIQ2
1175 P01B7 017D
```

```
1177                ********************************************************************
1178                *                                                                  *
1179                *                      PTP DATA A/Q COMMAND                        *
1180                *                                                                  *
1181                ********************************************************************


1182                PDT1    CJP     PTPDTJC,PDT2        JUMP IF PTP DATA STATUS
1183 P01B4 41B6
1184                        UJP     REJ1
1184 P01B5 0055
1185                PDT2    LDC     RAMADD,$0B
1185 P01B6 B40B
1186                        CA      AINUS,RAMD
1186 P01B7 C603
1187                        CA      AINLS,WCD
1187 P01B8 C802
1188                        CLO     RPLY
1188 P01B9 B3FF
1189                        LDC     RAMADD,$CC
1189 P01BA B40C
1190                PDT3    TA      WCS,RAMD
1190 P01BB C6F1
1191                        FFF     PTPDTFF
1191 P01C0 AF02
1192                        SFF     PTPIRFF
1192 P01C1 BF0A
1193                        RFF     PTPCA
1193 P01C2 AF35
1194                        UJP     MLP1
1194 P01C3 0056


1196                ********************************************************************
1197                *                                                                  *
1198                *                 PTP DEVICE FUNCTION A/Q COMMAND                  *
1199                *                                                                  *
1200                ********************************************************************


1202                PDF1    CJP     PTPDTJC,PDF2        JUMP IF PTP DATA STATUS
1202 P01C4 41C6
1203                        UJP     REJ1
1203 P01C5 0055
1204                PDF2    SFF     PARSUP
1204 P01C6 BF18
1205                        CA      AINLS,WCD
1205 P01C7 C802
```

```
1207                    SFEQL   PTPCA,RPLY
1207 P01C4 3335
1208                    RFF     PTPDTFF
1208 P01C6 AF02
1209                    SFF     PTPPAR
1209 P01CA BF1C
1210                PDF3    CJP     PARLTC,PDF4             JUMP IF PARITY LATCHED
1210 P01CF 6BCD
1211                    RFF     PTPPAR
1211 P01CC AF1C
1212                PDF4    LDC     RAMADD,$0A
1212 P01CD B40A
1213                    LDC     RAMD,$80                SET PTP INDEX CA
1213 P01CF B680
1214                    RFF     PARSUP
1214 P01CF AF1B
1215                    UJP     MLP1
1215 P01D0 0056


1217                ********************************************************************
1218                *                                                                  *
1219                *          PTP DISASSEMBLY TRANSFER STATUS A/Q COMMAND              *
1220                *                                                                  *
1221                ********************************************************************


1223                PDS1    LDC     AOUTLD,01
1223 P01D1 8C01
1224                    CJP     PTPDSJC,PDS2
1224 P01D2 3904
1225                    LDC     AOUTLD,00
1225 P01D3 8C00
1226                PDS2    CLO     RPLY
1226 P01D4 83FF
1227                    UJP     MLP1
1227 P01D5 0056


1229                ********************************************************************
1230                *                                                                  *
1231                *                      CP FEED A/Q COMMAND                         *
1232                *                                                                  *
1233                ********************************************************************


1235                CFD1    CJP     CPRDY,CFD2              JUMP IF CP READY
1235 P01D6 5FD8
```

```
1237                        UJP     REJ1
1237 P01D7 0055
1238                CFD2    CJP     CPPUIH,REJ1         JUMP IF CP PUNCH INHIBIT
1238 P01D8 7255
1239                        CJP     CPHOEM,REJ1         JUMP IF CP HOPPER EMPTY
1239 P01D9 6E55
1240                        RFFCL   CPDATFF,CPFEST      RESET CP DATA,SET CP FEED
1240 P01DA AE30
1241                        CLO     RPLY
1241 P01DB B3FF
1242                        UJP     MLP1
1242 P01DC 0056


1244                ********************************************************************
1245                *                                                                  *
1246                *                    CP CLEAR A/Q COMMAND                          *
1247                *                                                                  *
1248                ********************************************************************


1250                CCL1    RFFCL   CPDATFF,CPFIRT      RESET CP DATA,RESET CP FEED
1250 P01DD A430
1251                *                                    AND CP INFO READY
1252                        RFFCL   CPOFFS,RPLY         RESET CP OFFSET,SET REPLY
1252 P01DE A314
1253                        UJP     MLP1
1253 P01DF 0056


1255                ********************************************************************
1256                *                                                                  *
1257                *          CP INTERRUPT REQUEST A/Q COMMAND                        *
1258                *                                                                  *
1259                ********************************************************************


1261                CIQ1    LDC     RAMADD,6
1261 P01E0 8406
1262                        UJP     RIQ2
1262 P01E1 017D
```

```
1264                ********************************************************************
1265                *                                                                  *
1266                *                    CP OFFSET A/Q COMMAND                         *
1267                *                                                                  *
1268                ********************************************************************


1270                CDF1    TB      AINLS,BRCBD
1270 P01E2 0FF2
1271                        RFECL   CPOFFS,RPLY
1271 P01E3 A314
1272                        COF     BRSS,MLP1
1273 P01E4 5056
1273                        SFF     CPOFFS
1273 P01E5 8F14
1274                        UJP     MLP1
1274 P01E6 0055


1276                ********************************************************************
1277                *                                                                  *
1278                *                    CP DATA A/Q COMMAND                           *
1279                *                                                                  *
1280                ********************************************************************


1282                CDT1    CJP     CPDATJC,CDT2            JUMP IF CP DATA STATUS
1282 P01E7 21E9
1283                        UJP     REJ1
1283 P01E8 0055
1284                CDT2    CA      AINLS,CWALD
1284 P01E9 CA02
1285                        CA      AINUS,CWAUD
1285 P01EA CB03
1286                        CLC     CPINST                  SET CP INFO READY
1286 P01EB 56FF
1287                        RFECL   CPDATFF,RPLY            RESET CP DATA,SET REPLY
1287 P01EC A330
1288                        UJP     MLP1
1288 P01ED 0056
1289                        SPARE
1289 P01EE FFFF
1290                        SPARE
1290 P01EF FFFF
1291                        SPARE
1291 P01F0 FFFF
1292                        SPARE
1292 P01F1 FFFF
```

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1294                        SPARE
1294 P01F2 FFFF
1295                        SPARE
1295 P01F3 FFFF
1296                        SPARE
1296 P01F4 FFFF
1297                        SPARE
1297 P01F5 FFFF
1298                        SPARE
1298 P01F6 FFFF
1299                        SPARE
1299 P01F7 FFFF
1300                        SPARE
1300 P01F8 FFFF
1301                        SPARE
1301 P01F9 FFFF
1302                        SPARE
1302 P01FA FFFF
1303                        SPARE
1303 P01FB FFFF
1304                        SPARE
1304 P01FC FFFF
1305                        SPARE
1305 P01FD FFFF
1306                        SPARE
1306 P01FE FFFF
1307                        SPARE
1307 P01FF FFFF
1308              ************************************************************
1309              *                                                          *
1310              *              CP CLEAR INTERRUPT A/Q COMMAND              *
1311              *                                                          *
1312              ************************************************************


1314              CCI1    CLO     RPLY
1314 P0200 B3FF
1315                      RFF     RMBNKS
1315 P0201 AF33
1316                      LDC     RAMADD,6
1316 P0202 8406
1317                      LDC     RAMD,00             RESET CP INTERRUPT REQUESTS
1317 P0203 8600
1318                      LDC     RAMADD,3
1318 P0204 8403
1319                      LDC     RAMD,00             RESET CP INTERRUPT RESPONSE
1319 P0205 8600
1320                      LDC     RAMADD,1
1320 P0206 8401
1321              CCI2    TA      RAMS,BREGD
1321 P0207 CFF0
```

```
1323                    CJP     NOSE,PLP1       JUMP IF PTR INTRPT RESPONSE
1323 P021C [illegible]
1324                    LDC     PARADD,2
1324 P021E 8402
1325                    TA      RAMS,BREGD
1325 P0220 CFE0
1326                    CJP     NOSE,PLP1       JUMP IF PTR INTRPT RESPONSE
1326 P0222 [illegible]
1327                    RFF     INTRSP          RESET INTERRUPT RESPONSE
1327 P0224 BF2B
1328                    UJP     PLP1
1328 P0226 [illegible]
1329                ********************************************************************
1330                *                                                                  *
1331                *                          DELAY , INTERNAL                        *
1332                *                                                                  *
1333                *       THIS PROGRAM GENERATES A DELAY OF ABOUT 1 SECOND.           *
1334                *       USED WHEN ENTERING THE OFF-LINE CONDITION.                 *
1335                *                                                                  *
1336                ********************************************************************

1338                DLY1    RFF     PTPCUFF
1338 P0228 BF34
1339                        LDC     BF2LD,00
1339 P022A 5000
1340                        SFF     ENDLCK
1340 P022C BF19
1341                        SFF     ENDLOP
1341 P022E BF13
1342                        SFF     CNALU
1342 P0230 BF20
1343                DLY2    LDC     BREGD,$FF
1343 P0232 8FFF
1344                DLY3    COMPR   BREGS,BF2LS
1344 P0234 E36C
1345                        CJP     EQUAL,DLY6      JUMP IF B REGISTER EMPTY
1345 P0236 1E1B
1346                        LDC     WCD,$FF
1346 P0238 88FF
1347                DLY4    CJP     WCEMPT,DLY4     JUMP IF WC NOT EMPTY
1347 P023A 3017
1348                        DA      BREGS,BREGD     DECREMENT B REGISTER
1348 P023C CFFC
1349                DLY5    CJP     ONOFLN,CLC1     JUMP IF ON LINE
1349 P023E 465A
1350                        UJP     DLY3
1350 P0240 0014
1351                DLY6    CJP     PTPCUJC,DLY7
1351 P0242 241E
```

```
1353                        SFF     PTPCUFF
1353 P021C BF34
1354                        UJP     DLY2
1354 P021D 0013
1355                DLY7    RFF     CNALU
1355 P021E AF20
1356                        RFF     PTPCUFF
1356 P021F AF34
1357                        RFF     ENDLOP
1357 P0220 AF18
1358                        UJP     OFF1
1358 P0221 0022

1360                ********************************************************************
1361                *                                                                  *
1362                *       SELECT OFF-LINE MAINTENANCE ROUTINE , INTERNAL             *
1363                *                                                                  *
1364                *       THIS PROGRAM SELECTS THE CORRECT MAINTENANCE ROUTINE       *
1365                *       ACCORDING TO POSITION OF MAINTENANCE SWITCHES.             *
1366                *                                                                  *
1367                ********************************************************************

1369                OFF1    SFF     JGRP=
1369 P0222 BF29
1370                        CJP     MSW1,OFF6
1370 P0223 0830
1371                        CJP     MSW2,OFF5
1371 P0224 142D
1372                        CJP     MSW3,OFF4
1372 P0225 102B
1373                OFF2    RFF     JGRP9
1373 P0226 AF29
1374                        CJP     ONOFLN,OFF3         JUMP IF ON LINE
1374 P0227 4629
1375                        UJP     OFF2
1375 P0228 0026
1376                OFF3    RFF     RMBNKS
1376 P0229 AF33
1377                        UJP     CLCI
1377 P022A 005A
1378                OFF4    RFF     JGRP9
1378 P022B AF29
1379                        UJP     OCOI                OFF LINE CP ALL ONES
1379 P022C 00A6
1380                OFF5    CJP     MSW3,OFF2
1380 P022D 1026
1381                        RFF     JGRP9
1381 P022E AF29
1382                        UJP     ORBI                OFF LINE PTR BACKWARD MOTION
1382 P022F 0045
```

```
1384                OFF6    CJP     *SW2,OFF8
1384 P0230 1438
1385                        CJP     *SW3,OFF7
1385 P0231 1034
1386                        REF     JGRP9
1386 P0232 AF29
1387                        CJP     ORF1                    OFF LINE PTR FORWARD MOTION
1387 P0233 0039
1388                OFF7    REF     JGRP9
1388 P0234 AF29
1389                        UJP     OCT1                    OFF LINE CP TRIANGLE PUNCHING
1389 P0235 0063
1390                OFF8    CJP     *SW3,OFF2
1390 P0236 1026
1391                        REF     JGRP9
1391 P0237 AF29
1392                        CJP     OPP1                    OFF LINE PTP TRIANGLE PUNCHNG
1392 P0238 0047

1394                ********************************************************************
1395                *                                                                  *
1396                *                    OFF-LINE PTR FORWARD MOTION                   *
1397                *                                                                  *
1398                ********************************************************************

1400                ORF1    CJP     PTRSO,ORF2
1400 P0239 743B
1401                        UJP     OFF2
1401 P023A 0026
1402                ORF2    CJP     PTRSC,ORF5
1402 P023B 7040
1403                        SFF     PTRAC
1403 P023C AF21
1404                ORF3    CJP     PTR*,ORF3
1404 P023D 7040
1405                ORF4    CJP     PTR*C,ORF6
1405 P023E 7443
1406                        UJP     OFF2
1406 P023F 0026
1407                ORF5    REF     PTRAC
1407 P0240 AF21
1408                        CJP     ONOFLN,OFF3             JUMP IF ON LINE
1408 P0241 4629
1409                        UJP     ORF1
1409 P0242 0039
1410                ORF6    CJP     ONOFLN,OFF3
1410 P0243 4629
```

```
1412                        UJP     ORF3
1412 P0244 003D

1414                ********************************************************************
1415                *                                                                  *
1416                *                  OFF-LINE PTR BACKWARD MOTION                    *
1417                *                                                                  *
1418                ********************************************************************

1420                ORB1    SFF     PTRAM
1420 P0245 BF25
1421                        UJP     ORF1
1421 P0246 0039
1422                ********************************************************************
1423                *                                                                  *
1424                *                  OFF-LINE PTP TRIANGLE PUNCHING                  *
1425                *                                                                  *
1426                ********************************************************************

1428                OPP1    LDC     BF2UD,$FF
1428 P0247 BEFF
1429                OPP2    LDC     WCD,00
1429 P0248 8800
1430                        SFF     PTPPAR
1430 P0249 BF1C
1431                OPP3    CJP     PTPAO,OPP4
1431 P024A 784C
1432                        UJP     OFF2
1432 P024B 0026
1433                OPP4    CJP     PTPAC,OPP6
1433 P024C 7C4F
1434                OPP5    CJP     ONOFLN,OFF3
1434 P024D 4629
1435                        UJP     OPP3
1435 P024E 004A
1436                OPP6    CJP     PTPAM,OFF2
1436 P024F 6C26
1437                        SFF     PTPSCFF
1437 P0250 BF24
1438                OPP7    CJP     PTPAC,OPP10
1438 P0251 7C5F
1439                        RFF     PTPSCFF
1439 P0252 AF24
1440                        CJP     ONOFLN,OFF3
1440 P0253 4629
```

```
1443                    OFF5    SFF     CMALU
1443 P0254 4F20
1443                            COMPP   WCS*HF2US
1443 P0256 F3C9
1444                            HFF     CMALU
1444 P0258 4F20
1445                            HFF     PARSUP
1445 P025A 0071
1446                            CJP     EQUAL,OPP2
1446 P025C 1C48
1447                            LSFT    WCS,BREGL
1447 P025E 1EC9
1448                    OPP4    TA      BREGS,WCD
1448 P0260 C0FA
1449                            SFF     PTPPAR
1449 P0262 4F1C
1450                            CJP     PARLTC,OPP3
1450 P0264 5A40
1451                            SFF     PTPPAR
1451 P0266 4F1C
1452                            CJP     OPP3
1452 P0268 0044
1453                    OPP10   CJP     PTPAD,OPP11
1453 P026A 7FB1
1454                            CJP     OFF2
1454 P026C 0028
1455                    OPP11   CJP     ONOFLN,OFF3
1455 P026E 4F2C
1456                            CJP     OPP7
1456 P0270 0051
```

```
1458                    ********************************************************************
1459                    *                                                                  *
1460                    *                    OFF-LINE OR TRIANGLE PUNCHING                 *
1461                    *                                                                  *
1462                    ********************************************************************
```

```
1464                    OCT1    RFF     PTPDSFF
1464 P0272 4F32
1465                    OCT2    LDC     WCD,1
1465 P0274 0001
1466                            LDC     HF2LD,$50
1466 P0276 0050
1467                            LDC     HF2UD,$FF
1467 P0278 00FF
1468                            LDC     PAMADD,1
1468 P027A 0401
```

```
1470                    OCT3    LDC     RAMD,0
1470 P0268 8600
1471                            LDC     RFLGD,0
1471 P0269 8F00
1472                    OCT4    CJP     CPRDY,OCT5
1472 P026A 5E6C
1473                            UJP     OFF2
1473 P026B 0026
1474                    OCT5    CJP     CPPUIm,OFF2
1474 P026C 7226
1475                    OCT6    CJP     CPINFJC,OCT26
1475 P026D 52A2
1476                    OCT7    CJP     CPFEDJC,OCT24
1476 P026E 4A9E
1477                    OCT8    CJP     CPBSY,OCT9
1477 P026F 4271
1478                            UJP     OCT22
1478 P0270 009A
1479                    OCT9    CJP     PTPDSJC,OCT21
1479 P0271 3897
1480                            TA      BREGS,CWALD
1480 P0272 CAF4
1481                            TA      RAMS,CWAUD
1481 P0273 C8F0
1482                    OCT10   CLO     CPINST
1482 P0274 B6FF
1483                    OCT11   CJP     CPINFJC,OCT19
1483 P0275 5293
1484                            CJP     CPECER,OFF2
1484 P0276 6A26
1485                    OCT12   SFF     CNALU
1485 P0277 BF20
1486                            COMPR   WCS,BF2LS
1486 P0278 E369
1487                            RFF     CNALU
1487 P0279 AF20
1488                            CJP     EQUAL,OCT15
1488 P027A 1E8C
1489                            IA      WCS,BF2UD
1489 P027B CE09
1490                            TB      BF2US,WCD
1490 P027C F8A0
1491                            LDC     BF2UD,$FF
1491 P027D 8EFF
1492                            SFF     CNALU
1492 P027E BF20
1493                    OCT13   COMPR   BREGS,BF2US
1493 P027F F36C
1494                            RFF     CNALU
1494 P0280 AF20
1495                            CJP     EQUAL,OCT14
1495 P0281 1E84
1496                            LSFTI   BREGS,BREGD
```

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1496 P0295 CFCC
1497                    CJP     [illegible]
1497 P0297 [illegible]
1498                OCT14 LDC     [illegible]
1498 P0298 4E0F
1499                    SFF     CWALD
1499 P029[illegible]
1500                    CJP     [illegible]
1500 P029[illegible]
1501                    RFF     CWALD
1501 P029[illegible]
1502                    LDC     RF200,$FF
1502 P029[illegible]
1503                    CJP     [illegible]
1503 P029[illegible]
1504                    LSFTI   RAMS,RFF0
1504 P029A CBCB
1505                    CJP     OCT4
1505 P029[illegible]
1506                OCT15 CLC     CPFEST
1506 P029C 4FFF
1507                OCT16 CJP     CPFE,UC,OCT17
1507 P029E 4A8F
1508                    CJP     OFF2
1508 P02A[illegible]
1509                OCT17 CJP     CPRDY,OCT18
1509 P02A[illegible]
1510                    CJP     OFF2
1510 P02A[illegible]
1511                OCT18 CJP     ONUFLN,OFF3
1511 P02A[illegible]
1512                    CJP     OCT16
1512 P02A[illegible]
1513                OCT19 CJP     CPRDY,OCT20
1513 P02A[illegible]
1514                    CJP     OFF2
1514 P02A[illegible]
1515                OCT20 CJP     ONCFLT,OFF3
1515 P02A[illegible]
1516                    CJP     OCT11
1516 P02A[illegible]
1517                OCT21 LDC     CWALD,$FF
1517 P02A[illegible]
1518                    LDC     CWAUD,$0F
1518 P02A[illegible]
1519                    CJP     OCT10
1519 P02A[illegible]
1520                OCT22 CJP     CPRDY,OCT23
1520 P02A[illegible]
1521                    CJP     OFF2
1521 P02A[illegible]
1522                OCT23 CJP     ONUFLN,OFF3
1522 P02A[illegible]
```

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1523                        UJP     OCT5
1523 P02A5 006F
1524                OCT24   CJP     CPRDY,OCT25
1524 P02A6 5EA0
1525                        UJP     OFF2
1525 P02A7 0026
1526                OCT25   CJP     ONOFLN,OFF3
1526 P02A8 4629
1527                        UJP     OCT7
1527 P02A9 006E
1528                OCT26   CJP     CPRDY,OCT27
1528 P02AA 5EA4
1529                        UJP     OFF2
1529 P02AB 0025
1530                OCT27   CJP     ONOFLN,OFF3
1530 P02AC 4629
1531                        UJP     OCT6
1531 P02AD 006D

1533                ********************************************************************
1534                *                                                                  *
1535                *                  OFF-LINE CP ALL ONES PUNCHING                   *
1536                *                                                                  *
1537                ********************************************************************

1539                OC01    SFF     PTPOSFF
1539 P02AE 8F32
1540                        UJP     OCT2
1540 P02AF 0064
1541                        SPARE
1541 P02B0 FFFF
1542                        SPARE
1542 P02B1 FFFF
1543                        SPARE
1543 P02B2 FFFF
1544                        SPARE
1544 P02B3 FFFF
1545                        SPARE
1545 P02B4 FFFF
1546                        SPARE
1546 P02B5 FFFF
1547                        SPARE
1547 P02B7 FFFF
1548                        SPARE
1548 P02B7 FFFF
1549                        SPARE
1549 P02B8 FFFF
1550                        SPARE
1550 P02B9 FFFF
```

```
                ********************************************************************
                *                                                                  *
                *                        TEST MODE COMMANDS                        *
                *                                                                  *
                *      ANY TIME A TEST MODE COMMAND IS ISSUED, THE CONTROLLER      *
                *      ENTERS A SPECIAL STATE.                                     *
                *      WHEN IN THE TEST STATE, THE CONTROLLER ACCEPTS ONLY         *
                *      TEST TYPE A/N COMMANDS AND REJECTS ANY OTHER INSTRUCTION    *
                *      (EXCEPT CLEAR CONTROLLER AND STATUS 1.                      *
                *      TO EXIT FROM THE TEST STATE, A CLEAR CONTROLLER A/N         *
                *      COMMAND MUST BE ISSUED.                                     *
                *                                                                  *
                ********************************************************************


                ********************************************************************
                *                                                                  *
                *                      SELF TEST 1 A/N COMMAND                     *
                *                                                                  *
                *                THIS FUNCTION TESTS THE CONTROLLER                *
                *                INTERNAL DATA PATHS AND ALU.                      *
                *                                                                  *
                ********************************************************************


                STA1    CA      AINUS.BREGD
                        CA      AINUS.BF2LD
                        CA      AINLS.BF2UD
                        TA      AINLS.CWAUD
                        SFECL   BUSY.RPLY
                        RFF     EOP
                STA2    SEF     CNALU
                        DA      BREGS.BREGD
                        LSFT    BREGS.BREGD
                        PLUS    BREGS.CWAUS.BREGD
                        RFF     CNALU
                        IA      BREGS.BREGD
```

```
1588                STA3    MINUS   BREGS,BF2LS,BREGD
1588 P02BE EF6C
1589                        ANDAB   BREGS,BF2US,BREGD
1589 P02BF FFB4
1590                        OR      BREGS,BF2LS,AOUTLD
1590 P02C0 ECE4
1591                        LDC     BREGD,$F1
1591 P02C1 9FF1
1592                STA4    TA      BREGS,RAMADD
1592 P02C2 C4F4
1593                        TB      BF2US,CWAUD
1593 P02C3 FBA0
1594                STA5    TB      CWAUS,CWALD
1594 P02C4 DAA0
1595                        TB      CWALS,WCD
1595 P02C5 C8A0
1596                        TA      WCS,BF2LD
1596 P02C6 CDF1
1597                        TB      BF2LS,RAMD
1597 P02C7 E6A0
1598                        IA      RAMS,BF2UD
1598 P02C8 CE08
1599                        IA      BREGS,BREGD
1599 P02C9 CF0C
1600                STA6    CJP     COUT,STA4
1600 P02CA 1AC2
1601                        LDC     RAMADD,00
1601 P02CB 8400
1602                        TB      BF2US,RAMD
1602 P02CC F6A0
1603                        TB      BF2US,AOUTUD
1603 P02CD F9A0
1604                        UJP     RET1
1604 P02CE 0174
1605                ********************************************************************
1606                *                                                                  *
1607                *                    SELF TEST 2 A/Q COMMAND                       *
1608                *                                                                  *
1609                *              THIS FUNCTION TESTS THE CONTROLLER                  *
1610                *              INTERNAL FLIP-FLOPS AND JUMP CONDITIONS.            *
1611                *                                                                  *
1612                ********************************************************************


1614                STB1    SFF     BUSY
1614 P02CF BF2E
1615                        RFFCL   EOP,RPLY
1615 P02D0 A303
1616                        RFF     PTPCUFF
1616 P02D1 AF34
1617                        RFF     PTPDSFF
1617 P02D2 AF32
```

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1619                            RFF     CPDATFF
1619 P02D3 AF30
1620                            RFF     PTPDTFF
1620 P02D4 AF2F
1621                    STB2    RFF     PTRAYFF
1621 P02D5 AF0C
1622                            RFF     PTPSTFF
1622 P02D6 AF0A
1623                            RFF     PTPBFFF
1623 P02D7 AF09
1624                            RFF     PTP1RFF
1624 P02D8 AF08
1625                             FFF     PTPSCFF
1625 P02D9 AF24
1626                            RFF     PTRBFFF
1626 P02DA AF06
1627                    STB3    RFF     PTPDYFF
1627 P02DB AF05
1628                            RFF     PTPDTFF
1628 P02DC AF02
1629                            RFF     PTRACFF
1629 P02DD AF01
1630                            CJP     PTPCDJC,STB9
1630 P02DF 24F9
1631                            CJP     PTPDSJC,STB9
1631 P02DF 38F9
1632                            CJP     CPDATJC,STB9
1632 P02E0 20F9
1633                    STB4    CJP     PTRDTJC,STB9
1633 P02E1 54F9
1634                            CJP     PTPAYJC,STB9
1634 P02E2 1CF9
1635                            CJP     PTPSTJC,STB9
1635 P02E3 10F9
1636                            CJP     PTRBEJC,STB9
1636 P02E4 18F9
1637                            CJP     PTP1RJC,STB9
1637 P02E5 14F9
1638                    STB5    CJP     PTPSCJC,STB9
1638 P02E6 34F9
1639                            CJP     PTRBFJC,STB9
1639 P02E7 4CF9
1640                            CJP     PTPDYJC,STB9
1640 P02E8 2CF9
1641                            CJP     PTPDTJC,STB9
1641 P02E9 40F9
1642                            CJP     PTRACJC,STB9
1642 P02EA 44F9
1643                    STB6    SFF     PTPCDFF
1643 P02EB BF34
1644                            SFF     PTPDSFF
1644 P02EC BF32
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1646                        SFF     CPDATFF
1646 P02ED BF30
1647                        SFF     PTRDTFF
1647 P02EE BF2F
1648                        SFF     PTRAYFF
1648 P02EF BF0C
1649                        SFF     PTPSTFF
1649 P02F0 BF0A
1650                STB7    SFF     PTRPEFF
1650 P02F1 BF09
1651                        SFF     PTPIRFF
1651 P02F2 BF08
1652                        SFF     PTPSCFF
1652 P02F3 BF24
1653                        SFF     PTRBFFF
1653 P02F4 BF06
1654                        SFF     PTPDYFF
1654 P02F5 BF05
1655                        SFF     PTPDTFF
1655 P02F6 BF02
1656                STB8    SFF     PTRACFF
1656 P02F7 BF01
1657                        CJP     PTPCUJC,STB10
1657 P02F8 24FC
1658                STB9    LDC     AOUTLD,$AD
1658 P02F9 8CAD
1659                        LDC     AOUTUD,$DE
1659 P02FA 89DE
1660                        UJP     RET1
1660 P02FB 0174
1661                STB10   CJP     PTPDSJC,STB11
1661 P02FC 38FE
1662                        UJP     STB9
1662 P02FD 00F9
1663                STB11   CJP     CPDATJC,STB12
1663 P02FE 2100
1664                        UJP     STB9
1664 P02FF 00F9
1665                STB12   CJP     PTRDTJC,STB13
1665 P0300 5502
1666                        UJP     STB9
1666 P0301 00F9
1667                STB13   CJP     PTRAYJC,STB14
1667 P0302 1D04
1668                        UJP     STB9
1668 P0303 00F9
1669                STB14   CJP     PTPSTJC,STB15
1669 P0304 1106
1670                        UJP     STB9
1670 P0305 00F9
1671                STB15   CJP     PTRPEJC,STB16
1671 P0306 1908
```

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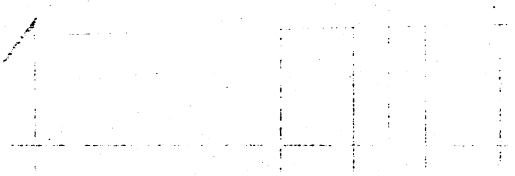
1673                            UJP     ST89
1673 P0307 00F9
1674                    STB16   CJP     PTPIPJC,STB17
1674 P0308 150A
1675                            UJP     ST89
1675 P0309 00F9
1676                    STB17   CJP     PTPSCJC,STB18
1676 P030A 350C
1677                            UJP     ST89
1677 P030B 00F9
1678                    STB18   CJP     PTRBFJC,STB19
1678 P030C 4D0E
1679                            UJP     ST89
1679 P030D 00F9
1680                    STB19   CJP     PTPOYJC,STB20
1680 P030E 2D10
1681                            UJP     ST89
1681 P030F 00F9
1682                    STB20   CJP     PTPOTJC,STB21
1682 P0310 4112
1683                            UJP     ST89
1683 P0311 00F9
1684                    STB21   CJP     PTRACJC,STB22
1684 P0312 4514
1685                            UJP     ST89
1685 P0313 00F9
1686                    STB22   SFF     ONBUSFF
1686 P0314 BF23
1687                    STB23   CJP     ONBUSJC,STB9
1687 P0315 3CF9
1688                            RFF     ONBUSFF
1688 P0316 AF23
1689                            CJP     ONBUSJC,STB24
1689 P0317 3D19
1690                            UJP     STB9
1690 P0318 00F9
1691                    STB24   CLO     CPFIRT
1691 P0319 B4FF
1692                            CJP     CPINFJC,STB9
1692 P031A 52F9
1693                            CJP     CPFEDJC,STB9
1693 P031B 4AF9
1694                    STB25   CLO     CPINST
1694 P031C B6FF
1695                            CLO     CPFEST
1695 P031D BEFF
1696                            CJP     CPINFJC,STB26
1696 P031E 5320
1697                            UJP     STB9
1697 P031F 00F9
1698                    STB26   CJP     CPFEDJC,STB27
1698 P0320 4822
```

```
1700                            UJP     ST89
1700 P0321 00F9
1701                    STB27   LDC     BREGD,$A5
1701 P0322 8FA5
1702                            LDC     CWALD,$A5
1702 P0323 8AA5
1703                    STB28   SFF     CWALU
1703 P0324 8F20
1704                            COMPR   BREGS,CWALS
1704 P0325 C36C
1705                            RFF     CWALU
1705 P0326 AF20
1706                            CJP     EQUAL,STB29
1706 P0327 1F29
1707                            UJP     ST89
1707 P0328 00F9
1708                    STB29   CJP     COUT,STB30
1708 P0329 1B28
1709                            UJP     ST89
1709 P032A 00F9
1710                    STB30   CJP     BMSB,STB31
1710 P0328 512D
1711                            UJP     ST89
1711 P032C 00F9
1712                    STB31   CJP     BMDL,STB32
1712 P032D 292F
1713                            UJP     STB9
1713 P032E 00F9
1714                    STB32   SFF     CWALLU
1714 P032F 8F20
1715                            PLUS    BREGS,CWALS,BREGD
1715 P0330 CF9C
1716                            RFF     CWALU
1716 P0331 AF20
1717                            CJP     COUT,ST89
1717 P0332 1AF9
1718                            CJP     BMDL,ST89
1718 P0333 28F9
1719                    STB33   CJP     BMSB,ST89
1719 P0334 50F9
1720                            LDC     AOUTLD,$ED
1720 P0335 8CED
1721                            LDC     AOUTUD,$AC
1721 P0336 89AC
1722                            UJP     RET1
1722 P0337 0174
```



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1724                ********************************************************************
1725                *                                                                  *
1726                *                      SELF TEST 3 A/Q COMMAND                     *
1727                *                                                                  *
1728                *              THIS FUNCTION DIRECTS THE CONTROLLER                *
1729                *              TO TEST THE DATA PATHS INTERCONNECTING              *
1730                *              THE CONTROLLER AND THE PT-RELAY STATION.            *
1731                *                                                                  *
1732                ********************************************************************


1734                STC1    CA      AINLS,WCD
1734 P0338 CB02
1735                        SFFCL   ECHO,RPLY
1735 P0339 B331
1736                        RFF     EOP
1736 P033A AF03
1737                        SFF     BUSY
1737 P033B BF2E
1738                        RFF     PTPSCFF
1738 P033C AF24
1739                        RFF     PTRAM
1739 P033D AF25
1740                STC2    RFF     PTRAC
1740 P033E AF21
1741                        RFF     PTPCA
1741 P033F AF35
1742                        RFFCL   PTPPAR,PTRRT
1742 P0340 A71C
1743                        CJP     PTRSC,STC13
1743 P0341 7160
1744                        CJP     PTPAM,STC13
1744 P0342 6D60
1745                        CJP     PTPAC,STC13
1745 P0343 7D60
1746                STC3    CLO     PTRRT
1746 P0344 B7FF
1747                        CJP     PTRCA,STC13
1747 P0345 6160
1748                        CJP     PTRPAR,STC13
1748 P0346 6560
1749                        SFF     PTPSCFF
1749 P0347 BF24
1750                        SFF     PTRAM
1750 P0348 BF25
1751                        SFF     PTRAC
1751 P0349 BF21
1752                        SFF     PTPCA
1752 P034A BF35
1753                STC4    SFFCL   PTPPAR,PTRRT
1753 P034B B71C
```

```
1755                          CJP     PTRSC,STC8
1755 P034C 7152
1756                  STC5    LDC     AOUTLD,$28
1756 P034D 8C28
1757                          LDC     AOUTUD,$14
1757 P034E 8914
1758                  STC6    RFF     ECHO
1758 P034F AF31
1759                  STC7    LDC     AOUTLD,00
1759 P0350 8C00
17760                          UJP     RET1
1760 P0351 0174
1761                  STC8    CJP     PTPAM,STC9
1761 P0352 6D54
1762                          UJP     STC5
1762 P0353 014D
1763                  STC9    CJP     PTPAC,STC10
1763 P0354 7D56
1764                          UJP     STC5
1764 P0355 014D
1765                  STC10   CLO     PTRRT
1765 P0356 B7FF
1766                          CJP     PTRCA,STC11
1766 P0357 6159
1767                          UJP     STC5
1767 P0358 014D
1768                  STC11   CJP     PTRPAR,STC12
1768 P0359 6558
1769                          UJP     STC5
1769 P035A 014D
1770                  STC12   SFF     SELBREG
1770 P035B BF2D
1771                          TA      BREGS,BREGD
1771 P035C CFF4
1772                          RFF     SELBREG
1772 P035D AF2D
1773                          TA      BREGS,AOUTUD
1773 P035E C9F4
1774                          UJP     STC6
1774 P035F 014F
1775                  STC13   LDC     AOUTLD,$41
1775 P0360 8C41
1776                          LDC     AOUTUD,$82
1776 P0361 8982
1777                          UJP     STC6
1777 P0362 014F
```

```
1774                ************************************************************
1775                *                                                          *
1776                *            TEST MODE LOAD RAM ADDRESS A/Q COMMAND        *
1777                *                                                          *
1778                *    THIS COMMAND IS USED TOGETHER WITH TEST MODE READ RAM  *
1779                *    COMMAND TO ALLOW CPU TO CHECK CONTENTS OF RAM REGISTERS*
1780                *                                                          *
1781                ************************************************************

1783                TLA1    CA      AINLS,RAMADD
1783 P0363 C402
1784                        CA      AINLS,BREGD
1784 P0364 CF02
1785                        CLO     RPLY
1785 P0365 83FF
1786                        IA      BREGS,BF2LD
1786 P0366 CD0C
1787                        UJP     RET1
1787 P0367 0174
1788                ************************************************************
1789                *                                                          *
1790                *            TEST MODE INTERRUPT REQUEST A/Q COMMAND       *
1791                *                                                          *
1792                ************************************************************

1794                TIR1    SFFCL   PTRPEFF,RPLY
1794 P0368 8309
1795                        UJP     RET1
1795 P0369 0174

1797                ************************************************************
1798                *                                                          *
1799                *            TEST MODE CLEAR INTERRUPT A/Q COMMAND         *
1800                *                                                          *
1801                ************************************************************

1803                TCI1    RFFCL   PTRPEFF,RPLY
1803 P036A A309
1804                        RFF     INTRSP
1804 P036B AF28
1805                        UJP     RET1
1805 P036C 0174
```

```
1812                ********************************************************************
1813                *                                                                  *
1814                *              TEST MODE A-OUT STATUS A/Q COMMAND                  *
1815                *                                                                  *
1816                ********************************************************************


1818                AOS1    CLO     RPLY
1818 P036D B3FF
1819                        UJP     RET1
1819 P036E 0174


1821                ********************************************************************
1822                *                                                                  *
1823                *                  TEST MODE READ RAM A/Q COMMAND                  *
1824                *                                                                  *
1825                *    THIS COMMAND IS USED TOGETHER WITH TEST MODE LOAD RAM          *
1826                *    ADDRESS COMMAND TO ALLOW CPU TO CHECK CONTENTS OF RAM REG.     *
1827                *                                                                  *
1828                ********************************************************************


1830                TRF1    TA      RAMS,AOUTLD
1830 P036F CCF0
1831                        TB      BF2LS,RAMADD
1831 P0370 E4A0
1832                        TA      RAMS,AOUTUD
1832 P0371 C9F0
1833                        CLO     RPLY
1833 P0372 B3FF
1834                        UJP     RET1
1834 P0373 0174
1835                ********************************************************************
1836                *                                                                  *
1837                *                  TEST MODE A/Q COMMAND HANDLING                  *
1838                *                                                                  *
1839                ********************************************************************


1841                RET1    CJP     PTRPEJC,RET2
1841 P0374 1976
1842                        UJP     RET3
1842 P0375 0177
1843                RET2    SFF     INTRSP
1843 P0376 BF28
```

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1845                    RET3    SFF     EOP
1845 P0377 BF03
1846                            RFF     BUSY
1846 P0378 AF2E
1847                    RET4    CJP     ONOFLN,RET5
1847 P0379 4778
1848                            UJP     OFF3
1848 P037A 0029
1849                    RET5    CJP     RMEXEC,RET6
1849 P037B 097D
1850                            UJP     RET4
1850 P037C 0179
1851                    RET6    CA      OS,*CD
1851 P037D C805
1852                            SFF     CNALU
1852 P037E BF20
1853                            LSFT    WCS,BREGD
1853 P037F CFC9
1854                            CJP     RMDL,RET8
1854 P0380 2984
1855                    RET7    CLO     PEJ
1855 P0381 B1FF
1856                            RFF     CNALU
1856 P0382 AF20
1857                            UJP     RET4
1857 P0383 0179
1858                    RET8    LSFT    BREGS,BREGD
1858 P0384 CFCC
1859                            CJP     RMDL,RET9
1859 P0385 2987
1860                            UJP     RET7
1860 P0386 0181
1861                    RET9    RFF     CNALU
1861 P0387 AF20
1862                            RFF     RMBNKS
1862 P0388 AF33
1863                            CA      OS,PCD
1863 P0389 C705
1864                            SPARE
1864 P038A FFFF
1865                            SPARE
1865 P038B FFFF
1866                            SPARE
1866 P038C FFFF
1867                            SPARE
1867 P038D FFFF
1868                            SPARE
1868 P038E FFFF
1869                            SPARE
1869 P038F FFFF
1870                            SPARE
1870 P0390 FFFF
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1872                    SPARE
1872 P0391 FFFF
1873                    SPARE
1873 P0392 FFFF
1874                    SPARE
1874 P0393 FFFF
1875                    SPARE
1875 P0394 FFFF
1876                    SPARE
1876 P0395 FFFF
1877                    SPARE
1877 P0396 FFFF
1878                    SPARE
1878 P0397 FFFF
1879                    SPARE
1879 P0398 FFFF
1880                    SPARE
1880 P0399 FFFF
1881                    SPARE
1881 P039A FFFF
1882                    SPARE
1882 P039B FFFF
1883                    SPARE
1883 P039C FFFF
1884                    SPARE
1884 P039D FFFF
1885                    SPARE
1885 P039E FFFF
1886                    SPARE
1886 P039F FFFF
1887                    SPARE
1887 P03A0 FFFF
1888                    SPARE
1888 P03A1 FFFF
1889                    SPARE
1889 P03A2 FFFF
1890                    SPARE
1890 P03A3 FFFF
1891                    SPARE
1891 P03A4 FFFF
1892                    SPARE
1892 P03A5 FFFF
1893                    SPARE
1893 P03A6 FFFF
1894                    SPARE
1894 P03A7 FFFF
1895                    SPARE
1895 P03A8 FFFF
1896                    SPARE
1896 P03A9 FFFF
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1898 SPARE
1898 P03AA FFFF
1899 SPARE
1899 P03AB FFFF
1900 SPARE
1900 P03AC FFFF
1901 SPARE
1901 P03AD FFFF
1902 SPARE
1902 P03AE FFFF
1903 SPARE
1903 P03AF FFFF
1904 SPARE
1904 P03B0 FFFF
1905 SPARE
1905 P03B1 FFFF
1906 SPARE
1906 P03B2 FFFF
1907 SPARE
1907 P03B3 FFFF
1908 SPARE
1908 P03B4 FFFF
1909 SPARE
1909 P03B5 FFFF
1910 SPARE
1910 P03B6 FFFF
1911 SPARE
1911 P03B7 FFFF
1912 SPARE
1912 P03B8 FFFF
1913 SPARE
1913 P03B9 FFFF
1914 SPARE
1914 P03BA FFFF
1915 SPARE
1915 P03BB FFFF
1916 SPARE
1916 P03BC FFFF
1917 SPARE
1917 P03BD FFFF
1918 SPARE
1918 P03BE FFFF
1919 SPARE
1919 P03BF FFFF
1920 SPARE
1920 P03C0 FFFF
1921 SPARE
1921 P03C1 FFFF
1922 SPARE
1922 P03C2 FFFF
1923 SPARE
1923 P03C3 FFFF

1925		SPARE
1925	P03C4 FFFF	
1926		SPARE
1926	P03C5 FFFF	
1927		SPARE
1927	P03C6 FFFF	
1928		SPARE
1928	P03C7 FFFF	
1929		SPARE
1929	P03C8 FFFF	
1930		SPARE
1930	P03C9 FFFF	
1931		SPARE
1931	P03CA FFFF	
1932		SPARE
1932	P03CB FFFF	
1933		SPARE
1933	P03CC FFFF	
1934		SPARE
1934	P03CD FFFF	
1935		SPARE
1935	P03CE FFFF	
1936		SPARE
1936	P03CF FFFF	
1937		SPARE
1937	P03D0 FFFF	
1938		SPARE
1938	P03D1 FFFF	
1939		SPARE
1939	P03D2 FFFF	
1940		SPARE
1940	P03D3 FFFF	
1941		SPARE
1941	P03D4 FFFF	
1942		SPARE
1942	P03D5 FFFF	
1943		SPARE
1943	P03D6 FFFF	
1944		SPARE
1944	P03D7 FFFF	
1945		SPARE
1945	P03D8 FFFF	
1946		SPARE
1946	P03D9 FFFF	
1947		SPARE
1947	P03DA FFFF	
1948		SPARE
1948	P03DB FFFF	
1949		SPARE
1949	P03DC FFFF	
1950		SPARE
1950	P03DD FFFF	

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1952                    SPARE
1952 P03DE FFFF
1953                    SPARE
1953 P03DF FFFF
1954                    SPARE
1954 P03E0 FFFF
1955                    SPARE
1955 P03E1 FFFF
1956                    SPARE
1956 P03E2 FFFF
1957                    SPARE
1957 P03E3 FFFF
1958                    SPARE
1958 P03E4 FFFF
1959                    SPARE
1959 P03E5 FFFF
1960                    SPARE
1960 P03E6 FFFF
1961                    SPARE
1961 P03E7 FFFF
1962                    SPARE
1962 P03E8 FFFF
1963                    SPARE
1963 P03E9 FFFF
1964                    SPARE
1964 P03EA FFFF
1965                    SPARE
1965 P03EB FFFF
1966                    SPARE
1966 P03EC FFFF
1967                    SPARE
1967 P03ED FFFF
1968                    SPARE
1968 P03EE FFFF
1969                    SPARE
1969 P03EF FFFF
1970                    SPARE
1970 P03F0 FFFF
1971                    SPARE
1971 P03F1 FFFF
1972                    SPARE
1972 P03F2 FFFF
1973                    SPARE
1973 P03F3 FFFF
1974                    SPARE
1974 P03F4 FFFF
1975                    SPARE
1975 P03F5 FFFF
1976                    SPARE
1976 P03F6 FFFF
1977                    SPARE
1977 P03F7 FFFF
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1979                    SPARE
1979 P03F8 FFFF
1980                    SPARE
1980 P03F9 FFFF
1981                    SPARE
1981 P03FA FFFF
1982                    SPARE
1982 P03FB FFFF
1983                    SPARE
1983 P03FC FFFF
1984                    SPARE
1984 P03FD FFFF
1985                    SPARE
1985 P03FE FFFF
1986                    SPARE
1986 P03FF FFFF
1987                  END     START1

PGM=  0400 (  1024)   COM = 0000 (     0)   DAT = 0000 (     0)
```

E Q U I V A L E N C E S

DFF.LINE	NAME	VALUE		REFFRENCED AT LINE NUMBER
0000	I	00FF	(000255)	
0243	MODE0	0000	(000000)	
0244	MODE1	0001	(000001)	
0245	MODE2	0002	(000002)	
0246	MODE3	0003	(000003)	
0247	MODE4	0004	(000004)	
0248	MODE5	0005	(000005)	
0250	MODE6	0006	(000006)	
0251	MODE7	0007	(000007)	
0252	MODE8	0008	(000008)	
0253	MODE9	0009	(000009)	
0254	MODEA	000A	(000010)	
0256	MODEB	000B	(000011)	
0257	MODEC	000C	(000012)	
0258	MODED	000D	(000013)	
0259	MODEE	000E	(000014)	
0260	MODEF	000F	(000015)	
0264	NU	0003	(000003)	
0265	RAMADD	0004	(000004)	0636, 0686, 0689, 0692, 0710, 0741, 0758, 0763, 0775, 0793, 0800, 0822, 0844, 0853, 0863, 0874 0881, 0910, 0917, 0971, 0985, 1000, 1025, 1028, 1041, 1044, 1046, 1049, 1060, 1073, 1084, 1147 1159, 1162, 1164, 1174, 1185, 1189, 1212, 1261, 1316, 1318, 1320, 1324, 1468, 1592, 1601, 1788 1831
0266	RANKD	0005	(000005)	
0267	RAMD	0006	(000006)	0638, 0742, 0774, 0779, 0784, 0801, 0848, 0882, 0919, 0972, 0974, 1026, 1029, 1042, 1045, 1061 1149, 1160, 1163, 1186, 1190, 1213, 1317, 1319, 1470, 1504, 1597, 1602
0268	PCD	0007	(000007)	0596, 1863
0269	WCD	0008	(000008)	0854, 1187, 1205, 1346, 1429, 1448, 1465, 1490, 1595, 1734, 1851
0270	AOUTUD	0009	(000009)	1075, 1603, 1659, 1721, 1757, 1773, 1776, 1832
0271	CWALD	000A	(000010)	1284, 1480, 1517, 1594, 1702
0272	CWAUD	000B	(000011)	1285, 1481, 1518, 1578, 1593
0273	AOUTLD	000C	(000012)	0500, 0502, 0511, 0513, 0522, 0524, 0533, 0535, 1074, 1087, 1090, 1100, 1102, 1223, 1225, 1590 1658, 1720, 1756, 1759, 1775, 1830
0274	BF2UD	000E	(000014)	0762, 0776, 1428, 1467, 1489, 1491, 1498, 1502, 1577, 1598
0275	BREGD	000F	(000015)	0635, 0639, 0687, 0690, 0693, 0711, 0739, 0759, 0764, 0794, 0823, 0845, 0875, 0911, 0969, 0986 0988, 1001, 1003, 1016, 1047, 1050, 1085, 1112, 1126, 1165, 1270, 1321, 1325, 1343, 1348, 1447 1471, 1496, 1575, 1582, 1583, 1584, 1586, 1588, 1589, 1591, 1599, 1701, 1715, 1771, 1789, 1853 1858
0276	BF2LD	000D	(000013)	1339, 1466, 1576, 1596, 1791

0280	RAMS	0000	(000000)	0687, 0690, 0693, 0711, 0759, 0764, 0776, 0794, 0823, 0845, 0854, 0875, 0911, 0986, 1001, 1047
				1050, 1074, 1085, 1165, 1321, 1325, 1481, 1500, 1504, 1598, 1830, 1832
0281	WCS	0001	(000001)	1190, 1443, 1447, 1486, 1489, 1596, 1853
0282	AINLS	0002	(000002)	0969, 0988, 1003, 1016, 1061, 1112, 1126, 1167, 1205, 1270, 1284, 1577, 1578, 1734, 1788, 1789
0283	AINUS	0003	(000003)	1186, 1285, 1575, 1576
0284	BREGS	0004	(000004)	0636, 0639, 0739, 0742, 1344, 1348, 1448, 1480, 1493, 1496, 1582, 1583, 1584, 1586, 1588, 1589
				1590, 1592, 1599, 1704, 1715, 1771, 1773, 1791, 1858
0285	QS	0005	(000005)	0596, 1851, 1863
0286	PCS	0007	(000007)	
0290	CWALS	0000	(000000)	1595, 1704, 1715
0291	CWAUS	0001	(000001)	1584, 1594
0292	BF2US	0003	(000003)	1075, 1443, 1490, 1493, 1500, 1589, 1593, 1602, 1603
0293	BF2LS	0002	(000002)	1344, 1486, 1588, 1590, 1597, 1831
0297	REJ	0001	(000001)	0600, 1855
0298	RPLY	0003	(000003)	0597, 0631, 0970, 0989, 1004, 1017, 1040, 1062, 1076, 1088, 1091, 1103, 1113, 1127, 1138, 1158
				1188, 1207, 1226, 1241, 1252, 1271, 1287, 1314, 1579, 1615, 1735, 1790, 1799, 1808, 1818, 1833
0299	CPFIRT	0004	(000004)	0671, 0956, 1250, 1691
0300	CPINST	0006	(000006)	1286, 1482, 1694
0301	PTRRT	0007	(000007)	0734, 1742, 1746, 1753, 1765
0302	PTPDYR	000C	(000012)	
0303	CPFEST	000E	(000014)	1240, 1506, 1695
0307	PTRSO	003A	(000058)	0714, 0795, 0930, 1400, 1405
0308	PTRSC	003B	(000056)	0716, 0732, 1402, 1404, 1743, 1755
0309	PTRACJ	0022	(000034)	0708, 0729, 1642, 1684
0310	PTRAYJ	000E	(000014)	0761, 0781, 1634, 1667
0311	PTRDTJ	002A	(000042)	0709, 0797, 1071, 1633, 1665
0312	PTRPAR	0032	(000050)	0736, 1748, 1768
0313	PTRCA	0030	(000048)	1747, 1766
0314	PTRPEJ	000C	(000012)	0760, 1101, 1636, 1671, 1841
0315	PTRBFJ	0026	(000038)	0728, 0756, 1639, 1678
0316	PTPAO	003C	(000060)	0876, 0943, 1431, 1453
0317	PTPAC	003E	(000062)	0816, 0840, 1433, 1438, 1745, 1763
0318	PTPAM	0036	(000054)	0820, 1436, 1744, 1761
0319	PTPSCJ	001A	(000026)	0819, 0842, 1638, 1676
0320	PTPSTJ	0008	(000008)	0813, 0837, 1125, 1635, 1669
0321	PTPDYJ	0016	(000022)	0825, 0851, 1640, 1680
0322	PTPDSJ	001C	(000028)	0828, 0861, 1224, 1479, 1631, 1661
0323	PTPDTJ	0020	(000032)	0878, 1183, 1202, 1641, 1682
0324	PTPCUJ	0012	(000018)	1351, 1630, 1657
0325	CPRSY	0021	(000033)	0900, 1477
0326	CPINFJ	0029	(000041)	0898, 1475, 1483, 1692, 1696
0327	CPECER	0035	(000053)	0512, 1484
0328	CPPUIH	0039	(000057)	0501, 0897, 0960, 1238, 1474
0329	CPRDY	002F	(000047)	0894, 0912, 0955, 1235, 1472, 1509, 1513, 1520, 1524, 1528
0330	CPSTHY	003D	(000061)	0523
0331	CPHOEM	0037	(000055)	0534, 1239
0332	CPFEDJ	0025	(000037)	0899, 1476, 1507, 1693, 1698
0333	CPDATJ	0010	(000016)	0914, 1282, 1632, 1663
0334	PARLTC	0034	(000052)	0743, 0856, 1210, 1450
0335	PTPIRJ	000A	(000010)	0821, 0843, 1637, 1674
0336	WCEMPT	001B	(000024)	1347
0337	ONOFLN	0023	(000035)	0612, 0674, 1349, 1374, 1408, 1410, 1434, 1440, 1455, 1511, 1515, 1522, 1526, 1530, 1847
0338	MSW1	0004	(000004)	1370

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0339    MSW2     000A    (000010)   1371, 1384
0340    MSW3     0008    (000008)   1372, 1380, 1385, 1390
0341    COUT     000D    (000013)   0640, 1600, 1708, 1717
0342    RMSB     002A    (000040)   0686, 0691, 0695, 0712, 0765, 0773, 0783, 0796, 0824, 0846, 0877, 0913, 0973, 0987, 1002, 1005
                                    1019, 1048, 1051, 1086, 1114, 1128, 1166, 1272, 1323, 1326, 1710, 1719
0343    RMDL     0014    (000020)   0804, 0885, 0922, 0990, 1018, 1712, 1718, 1854, 1859
0344    ONBUSJ   001E    (000030)   1687, 1689
0345    UNTPRT   0024    (000036)   0645
0346    EQUAL    000F    (000015)   1345, 1446, 1488, 1495, 1503, 1706
0347    RMEXEC   0004    (000004)   0614, 0629, 0697, 0719, 0730, 0771, 0798, 0814, 0838, 0879, 0895, 0915, 0934, 0946, 0958, 1849
0351    PTRAC    0021    (000033)   0654, 0717, 0769, 0932, 0975, 1022, 1403, 1407, 1740, 1751
0352    PTRACF   0001    (000001)   0655, 0718, 0770, 0933, 0976, 1023, 1629, 1656
0353    PTRAM    0025    (000037)   0656, 0989, 0991, 1024, 1420, 1739, 1750
0354    PTRAYF   000C    (000012)   0657, 1004, 1006, 1027, 1621, 1648
0355    PTRDTF   002F    (000047)   0658, 0767, 0931, 1030, 1076, 1620, 1647
0356    PTRPEF   0009    (000009)   0653, 0745, 1021, 1623, 1650, 1799, 1808
0357    PTRBFF   0006    (000006)   0659, 0746, 0768, 1031, 1626, 1653
0358    PTPSCF   0024    (000036)   0660, 0817, 0849, 0858, 0945, 1116, 1138, 1437, 1439, 1625, 1652, 1738, 1749
0359    PTPCA    0035    (000053)   0661, 1139, 1193, 1207, 1741, 1752
0360    PTPPAR   001C    (000028)   0662, 0855, 0857, 1140, 1209, 1211, 1430, 1449, 1451, 1742, 1753
0361    PTPSTF   000A    (000010)   0663, 1113, 1115, 1141, 1622, 1649
0362    PTPDSF   0032    (000050)   0666, 0862, 0865, 1143, 1464, 1539, 1617, 1644
0363    PTPDYF   0005    (000005)   0665, 1127, 1129, 1142, 1627, 1654
0364    PTPDTF   0002    (000002)   0667, 0826, 0944, 1144, 1191, 1208, 1628, 1655
0365    PTPIRF   0008    (000008)   0669, 0852, 1146, 1192, 1624, 1651
0366    PTPCUF   0034    (000052)   0668, 1145, 1338, 1353, 1356, 1616, 1643
0367    CPOFFS   0014    (000020)   0670, 1252, 1271, 1273
0368    CPDATF   0030    (000048)   0671, 0902, 0956, 1240, 1250, 1287, 1619, 1646
0369    CNALU    0020    (000032)   0632, 0642, 1342, 1355, 1442, 1444, 1485, 1487, 1492, 1494, 1499, 1501, 1581, 1585, 1703, 1705
                                    1714, 1716, 1852, 1856, 1861
0370    RMRNKS   0033    (000051)   0578, 0580, 0582, 0584, 0586, 0588, 0590, 0592, 0594, 0633, 0675, 1315, 1376, 1862
0371    SELRRE   002D    (000045)   0634, 0738, 0740, 1770, 1772
0372    ENDLCK   0019    (000025)   0649, 1340
0373    ONBUSF   0023    (000035)   0643, 1686, 1688
0374    ENDLOP   001B    (000027)   0648, 1341, 1357
0375    PARSUP   0018    (000024)   0650, 0734, 0737, 0747, 1204, 1214, 1445
0376    BUSY     002E    (000046)   0628, 0672, 1579, 1614, 1737, 1846
0377    JGRP9    0029    (000041)   0651, 1369, 1373, 1378, 1381, 1386, 1388, 1391
0378    INTRSP   0028    (000040)   0652, 0696, 0699, 0802, 0883, 0920, 1052, 1327, 1809, 1843
0379    CNTPRT   0000    (000000)   0644, 0646
0380    EOP      0003    (000003)   0673, 1580, 1615, 1736, 1845
0381    FCHO     0031    (000049)   0647, 1735, 1758
```

SYMBOLS

DEF.LINE	NAME	ADDRESS	REFERENCED AT LINE NUMBER
0382	START1	0000	0382, 0477, 0478, 0479, 0480, 0481, 0482, 0484, 0486, 0488, 0490, 0491, 0492, 0501, 0503, 0512 0514, 0523, 0525, 0534, 0536, 0537, 0538, 0539, 0540, 0543, 0545, 0546, 0547, 0548, 0549, 0550 0551, 0552, 0553, 0554, 0555, 0556, 0557, 0558, 0559, 0560, 0561, 0562, 0563, 0564, 0565, 0566 0567, 0568, 0569, 0572, 0574, 0576, 0577, 0579, 0581, 0583, 0585, 0587, 0589, 0591, 0593, 0595 0598, 0612, 0613, 0614, 0615, 0629, 0630, 0640, 0641, 0645, 0674, 0676, 0688, 0691, 0695, 0697 0698, 0700, 0708, 0709, 0712, 0713, 0714, 0715, 0716, 0719, 0720, 0728, 0729, 0730, 0731, 0732 0733, 0736, 0743, 0744, 0748, 0756, 0757, 0760, 0761, 0765, 0766, 0771, 0772, 0773, 0777, 0780 0781, 0782, 0783, 0785, 0795, 0796, 0797, 0798, 0799, 0803, 0804, 0805, 0813, 0814, 0815, 0816 0818, 0819, 0820, 0821, 0824, 0825, 0827, 0828, 0829, 0837, 0838, 0839, 0840, 0841, 0842, 0843 0846, 0847, 0850, 0851, 0856, 0860, 0861, 0864, 0866, 0876, 0877, 0878, 0879, 0880, 0884, 0885 0886, 0894, 0895, 0896, 0897, 0898, 0899, 0900, 0901, 0903, 0912, 0913, 0914, 0915, 0916, 0921 0922, 0923, 0930, 0934, 0935, 0943, 0946, 0947, 0955, 0958, 0959, 0960, 0961, 0973, 0977, 0987 0990, 0992, 1002, 1005, 1008, 1018, 1019, 1020, 1032, 1048, 1051, 1053, 1063, 1071, 1072, 1077 1086, 1089, 1092, 1101, 1104, 1114, 1117, 1125, 1128, 1130, 1150, 1166, 1167, 1175, 1183, 1184 1194, 1202, 1203, 1210, 1215, 1224, 1227, 1235, 1237, 1238, 1239, 1242, 1253, 1262, 1272, 1274 1282, 1283, 1288, 1323, 1326, 1328, 1345, 1347, 1349, 1350, 1351, 1354, 1358, 1370, 1371, 1372 1374, 1375, 1377, 1379, 1380, 1382, 1384, 1385, 1387, 1389, 1390, 1392, 1400, 1401, 1402, 1404 1405, 1406, 1408, 1409, 1410, 1412, 1421, 1431, 1432, 1433, 1434, 1435, 1436, 1438, 1440, 1446 1450, 1452, 1453, 1454, 1455, 1456, 1472, 1473, 1474, 1475, 1476, 1477, 1478, 1479, 1483, 1484 1488, 1495, 1497, 1503, 1505, 1507, 1508, 1509, 1510, 1511, 1512, 1513, 1514, 1515, 1516, 1519 1520, 1521, 1522, 1523, 1524, 1525, 1526, 1527, 1528, 1529, 1530, 1531, 1540, 1600, 1604, 1630 1631, 1632, 1633, 1634, 1635, 1636, 1637, 1638, 1639, 1640, 1641, 1642, 1657, 1660, 1661, 1662 1663, 1664, 1665, 1666, 1667, 1668, 1669, 1670, 1671, 1673, 1674, 1675, 1676, 1677, 1678, 1679 1680, 1681, 1682, 1683, 1684, 1685, 1687, 1689, 1690, 1692, 1693, 1696, 1697, 1698, 1700, 1706 1707, 1708, 1709, 1710, 1711, 1712, 1713, 1717, 1718, 1719, 1722, 1743, 1744, 1745, 1747, 1748 1755, 1760, 1761, 1762, 1763, 1764, 1766, 1767, 1768, 1769, 1774, 1777, 1792, 1800, 1810, 1819 1834, 1841, 1842, 1847, 1848, 1849, 1850, 1854, 1857, 1859, 1860
0478	START2	0001	0477
0500	CS21	000C	0488
0511	CS31	0010	0490
0522	CS41	0014	0491
0533	CS51	0018	0492
0578	CCI0	0040	0546
0580	ADS0	0042	0539
0582	TEM1	0044	0566
0584	TEM2	0046	0567
0586	TEM3	0048	0568
0588	TEM4	004A	0569
0590	TEM5	004C	0572
0592	TEM6	004E	0574
0594	TEM7	0050	0540

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0596    REX1    0052        0614, 0697, 0719, 0730, 0771, 0798, 0814, 0838, 0879, 0895, 0915, 0934, 0946, 0958
0597    REP1    0053        0501, 0503, 0512, 0514, 0523, 0525, 0534, 0536
0600    REJ1    0055        0479, 0480, 0537, 0538, 0556, 0557, 0565, 0576, 0577, 0987, 1002, 1072, 1125, 1184, 1203, 1237
                            1238, 1239, 1283
0612    MLP1    0056        0598, 0674, 0959, 0973, 0977, 0990, 0992, 1005, 1008, 1020, 1032, 1048, 1051, 1053, 1063, 1077
                            1089, 1092, 1104, 1114, 1117, 1128, 1130, 1150, 1166, 1194, 1215, 1227, 1242, 1253, 1272, 1274
                            1288, 1323, 1326, 1328
0614    MLP2    005B        0612
0628    CLC1    005A        0478, 0613, 1349, 1377
0631    CLC11   005D        0629
0632    CLC12   005E        0630
0636    CLC2    0062        0641
0639    CLC3    0064
0642    CLC4    0067        0640
0646    CLC5    006B
0647    CLC6    006C        0645
0652    CLC7    0071
0658    CLC8    0077
0665    CLC9    007D
0671    CLC10   0083
0686    ICM1    0089        0615
0692    ICM2    008F
0697    ICM3    0093        0700
0699    ICM4    0095        0688, 0691, 0695
0708    IAC1    0097        0698
0714    IAC2    009D        0712
0716    IAC3    009F        0714
0717    IAC4    00A0
0719    IAC5    00A2        0708, 0709, 0713, 0715, 0716
0728    IRT1    00A4        0720
0730    IRT2    00A6        0728, 0733, 0748
0732    IRT3    00A8        0729
0734    IRT4    00AA        0732
0737    IRT6    00AC
0738    IRT7    00AD        0736
0742    IRT8    00B1
0745    IRT9    00B4        0743
0746    IRT10   00B5        0744
0756    IRH1    00B8        0731
0758    IRH2    00BA        0756
0762    IRH3    00BE        0782
0763    IRH4    00BF        0780, 0785
0767    IRH5    00C3        0765
0768    IRH6    00C4        0777
0771    IRH7    00C7        0757, 0766
0773    IRH8    00C9        0761
0779    IRH9    00CE        0773, 0783
0781    IRH10   00D0        0760
0783    IRH11   00D2        0781
0793    IRI1    00D5        0772
0797    IRI2    00D9        0795
0798    IRI3    00DA        0803, 0805
0800    IRI4    00DC        0796, 0804
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0804	IRI5	00E0	0797
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COMMENT SHEET

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FE516-A PTR/PTP/CP Controller and DK609-A Paper Tape Relay Station

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